

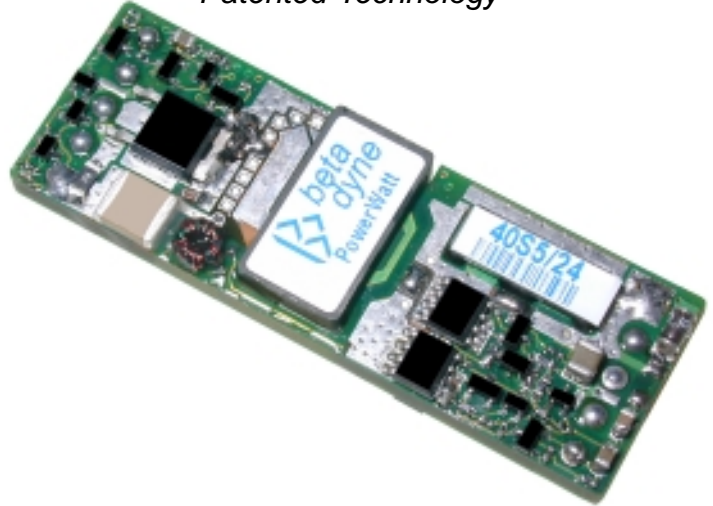


POWERWATT™ BD40000

40W SINGLE DC/DC CONVERTER
1/8-Brick package
Patented Technology

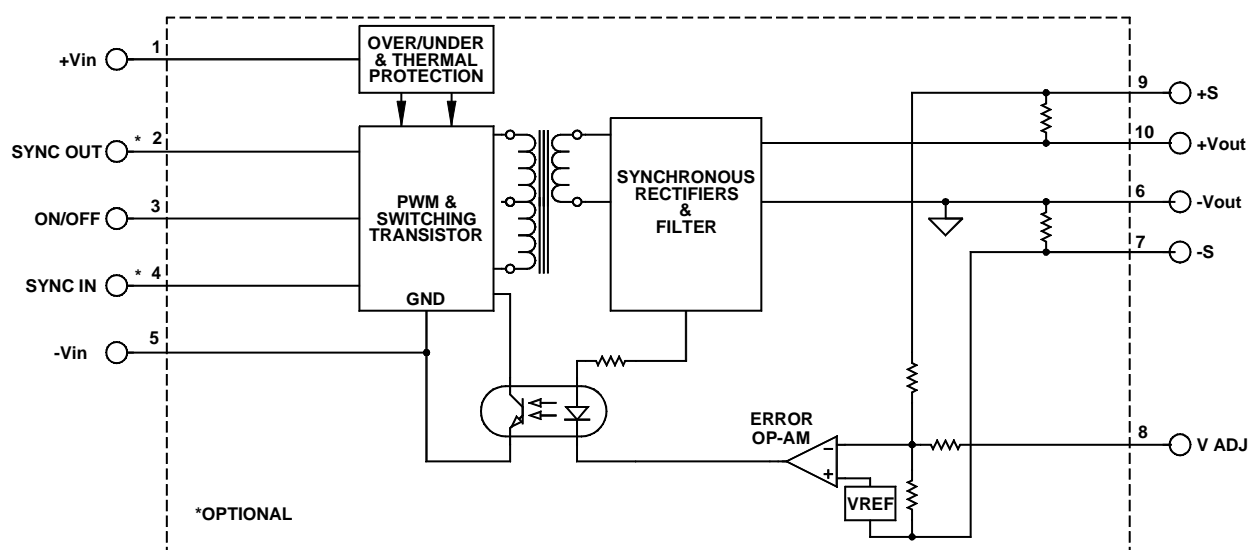
Key Features

- Efficiency up to 91%
- Power density of 60W/in³
- 25μS transient response time
- 150μA off state current
- Output synchronous rectification
- 2:1 input voltage range
- Input-to-output isolation
- Soft start
- External synchronization
- Short circuit protection
- Thermal protection
- Undervoltage protection
- Industry standard pinout



Functional Description

The BD40000 is derived from the 40W PowerWatt™ series and is designed to turn on at 41V and off between 38V and 39V. The converter features an industry standard pinout in a 2.3x0.78x0.38-inch 1/8-brick package. Patented technology coupled with SMD and planar magnetics makes it possible to offer a converter with 60W/in³ power density. A unique feature of the BD40000 is its transient response that approaches that of non-isolated step-down converters. Standard features include low input, off state current, and thermal and undervoltage protection.



Typical Block Diagram

Unless otherwise specified, all parameters are given under typical ambient temperature of +25°C with an airflow rate = 400LFM. With the given power derating, the operating range is -40°C to +125°C. Specifications subject to change without notice.

Electrical Specifications

INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Input Voltage Range	See Model Selection Guide	41	48	72	Vdc
Input Startup Voltage, $48V_{IN}$		38	39	41	Vdc
Undervoltage Shutdown, $48V_{IN}$				38	Vdc
Input Filter	Capacitor				
Reflected Ripple	See Model Selection Guide, Figure 2				
No Load Input Current	See Model Selection Guide				
Input Surge Current (20 μ S Spike)				10	A
Short Circuit Current Limit			125	150	% I_{IN} Max
Off State Current			150		μ A
Remote ON/OFF Control					
Supply ON	Pin 3 Open (Open circuit voltage: 10V Max.)				
Supply OFF		0		0.6	Vdc
Logic Input Reference	-Input pin 5 for On/Off, Sync In and Sync Out				
Logic Compatibility	TTL Open Collector or CMOS Open Drain				

OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Voltage and Current Ratings	See Model Selection Guide				
Output Voltage Accuracy			0.5	1	%
Output Voltage Adjustment	See also footnote 3 in Model Selection Guide		± 5		%
Ripple & Noise	Without external capacitor		1	2	% V_{PP} of V_{OUT}
Line Regulation	Minimum V_{IN} to maximum V_{IN}		± 0.2	± 0.5	%
Load Regulation	NL to FL		0.2	0.5	%
Temperature Coefficient @ FL			0.02		%/°C
Transient Response Time	50% FL to FL to 50% FL, See Figure 3		25	100	μ S
Short Circuit Protection	By input current limiting				
Turn On Delay with Soft Start	See Figure 4		3	4	mS
Output Overvoltage Protection	None, (See App. Note SR-001)				

GENERAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Efficiency (at full power)	See Model Selection Guide, Figures 1 & 5				
Isolation Voltage (1 min.), Input to Output	All models		1500		Vdc
Isolation Resistance			10^9		Ω
Isolation Capacitance			300		pF
Switching Frequency (F_s)		360	380	400	kHz
External Sync Frequency (F_e)	$F_e \leq F_s$, See External Synchronization	360	380	400	kHz

ENVIRONMENTAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Operating Temperature Range (Ambient)	Industrial, See Figure 6	-40		+71	°C
Storage Temperature Range		-55		+150	°C
Maximum Operating PCB Temperature				125	°C
Derating	See Figure 6				
Cooling	See Figure 6				
MTBF	per MIL-HNBK-217F (Ground benign, +25°C)		1.1×10^6		hours

PHYSICAL CHARACTERISTICS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Dimensions (LxWxH)	2.30x0.78x0.38 in. (58.42x19.80x9.65mm)				
Weight	0.765 oz. (23g)				

Model Selection Guide

MODEL NUMBER	INPUT				Reflected Ripple ² (mA _{PP})	OUTPUT		
	Voltage (Vdc)		Current (mA)			Voltage (Vdc)	Current (A)	Efficiency Full Load (%)
	Nominal	Range	No Load	Full Load ¹				
40S5/48	48	36-72	50	916	40	5	8	91

¹ The maximum input current at any given input range measured at minimum input voltage is given as $1.6 \cdot I_{\text{NOMINAL}}$. Nominal input current is the typical value measured at the input of the converter under full-load room temperature and nominal input voltage (24Vdc and 48Vdc).

² Measured with 22 μ F capacitor for 48V_{IN} and 100 μ F capacitor for 24V_{IN} at the input power pins in series with 10 μ H inductor (see Figure 2A).

ORDERING GUIDE

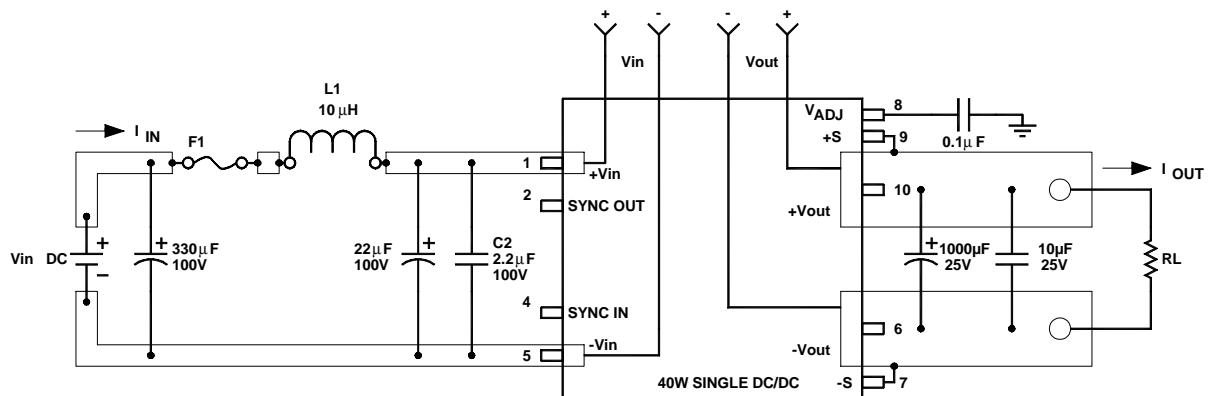
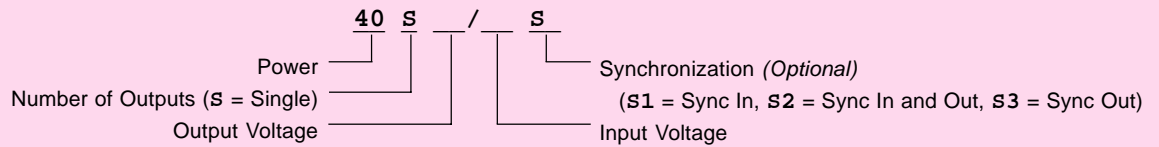


FIGURE 1. Setup for efficiency measurements

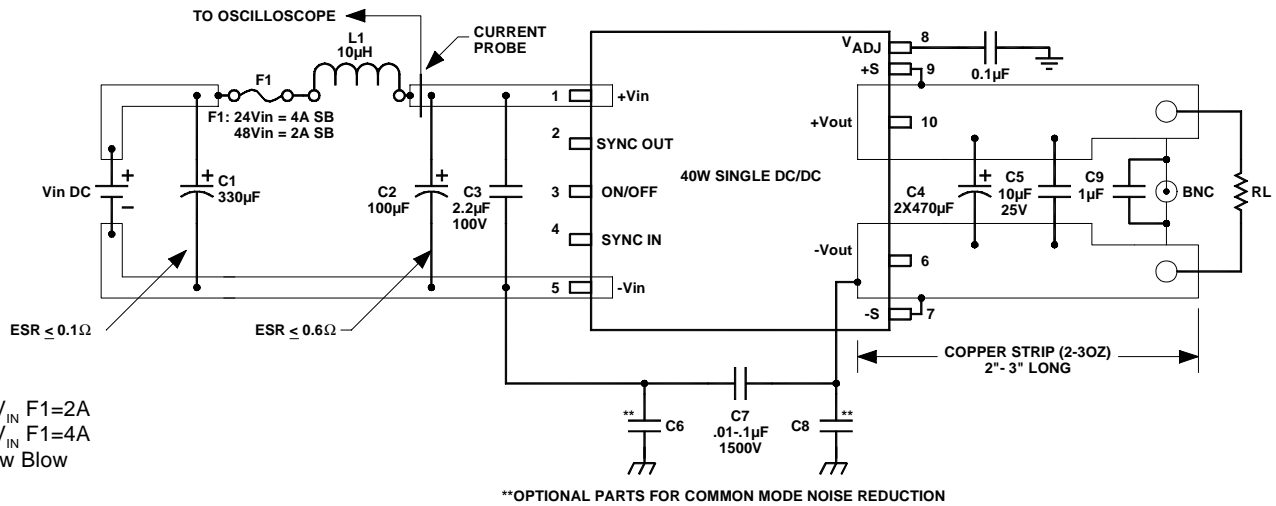


FIGURE 2A. Setup for output and reflected ripple measurement

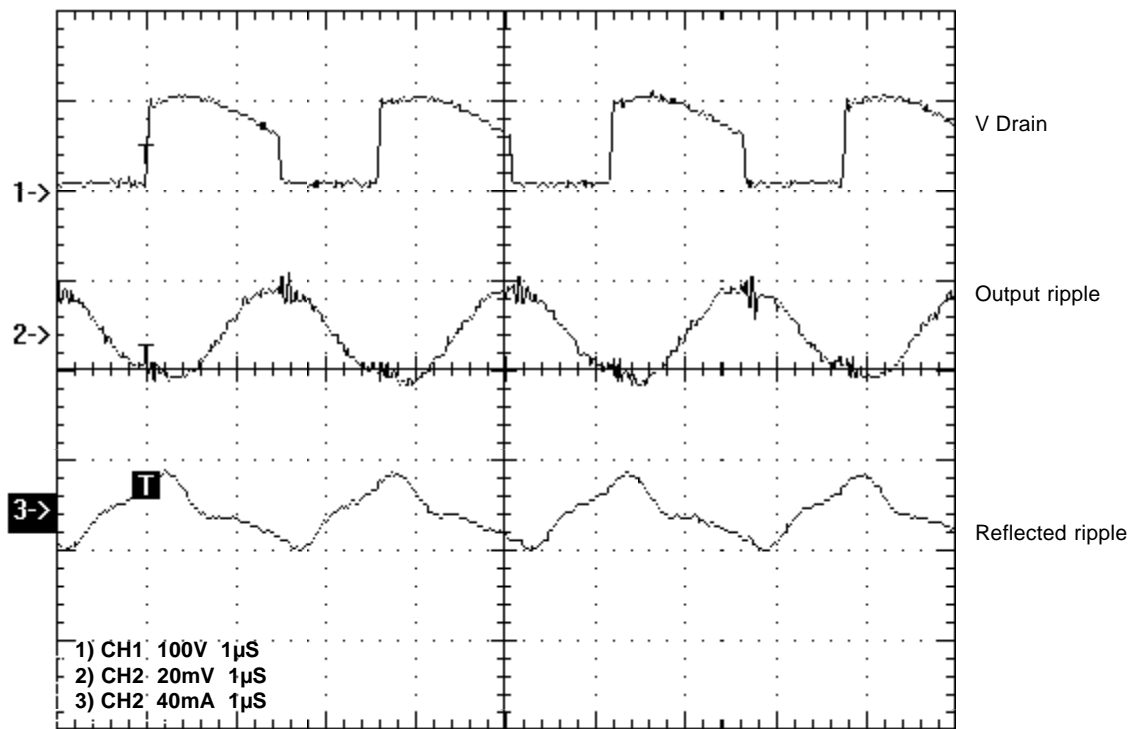


FIGURE 2B. Output ripple and reflected ripple from setup in Figure 2A for 40S3.3/24

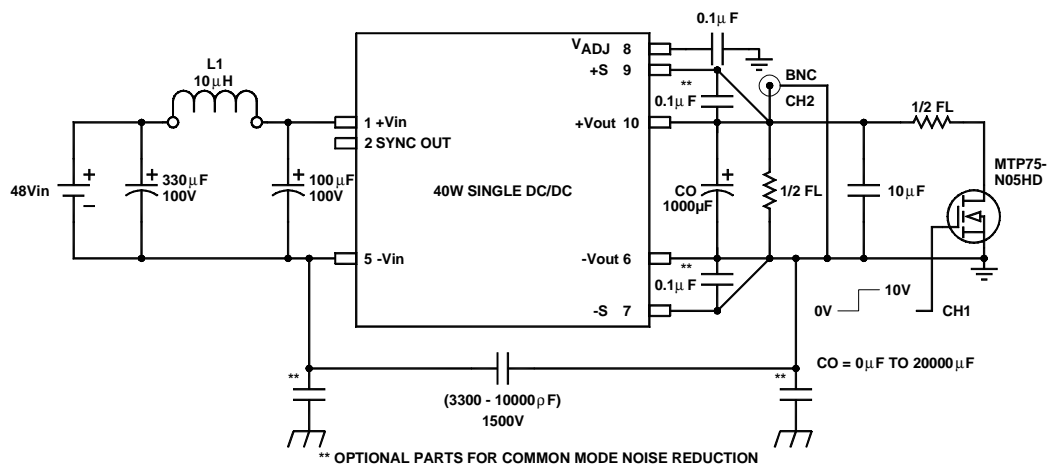


FIGURE 3A. Setup for transient response measurements

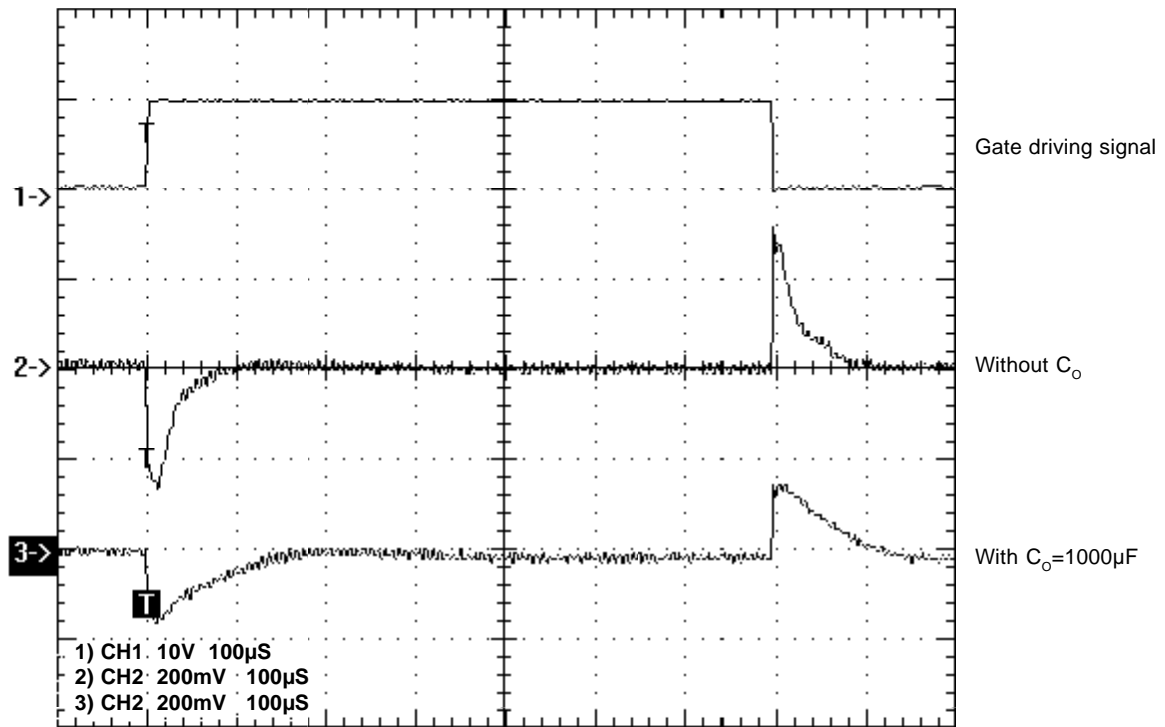


FIGURE 3B. Transient response of 40S3.3/48, 50% FL to FL load step

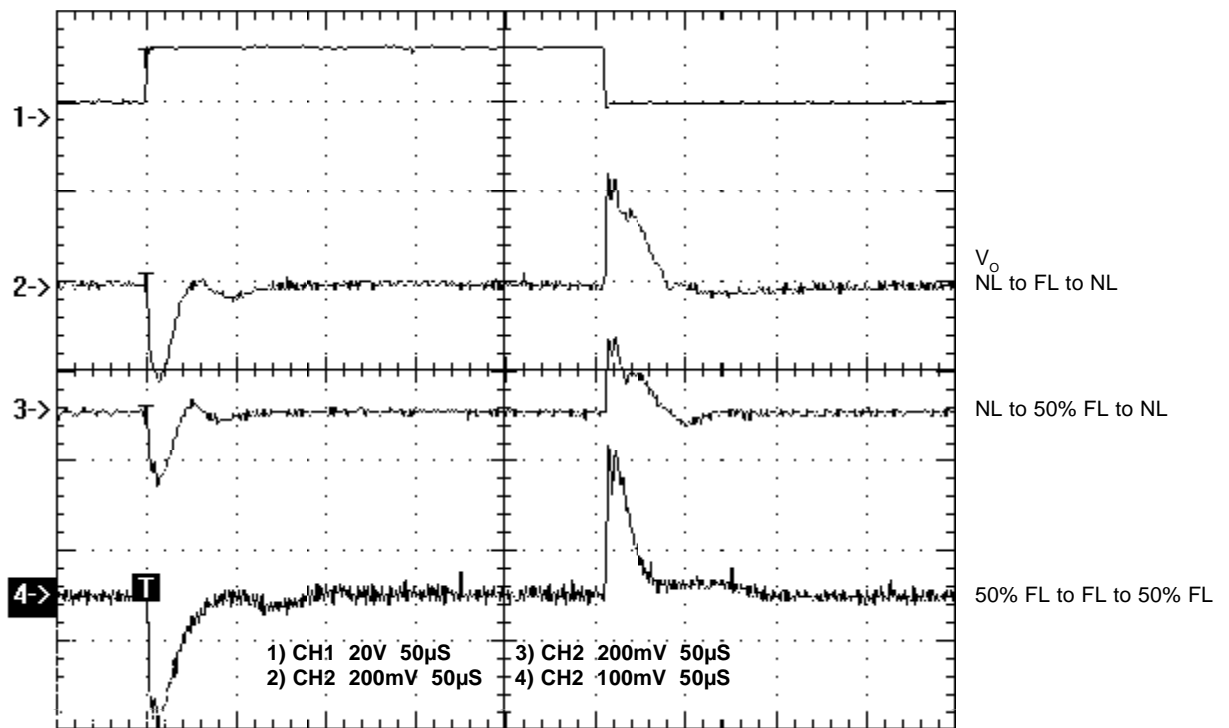


FIGURE 3C. Transient response with 1000µF capacitor with both sense pins connected at the load
(Refers to Figure 3A)

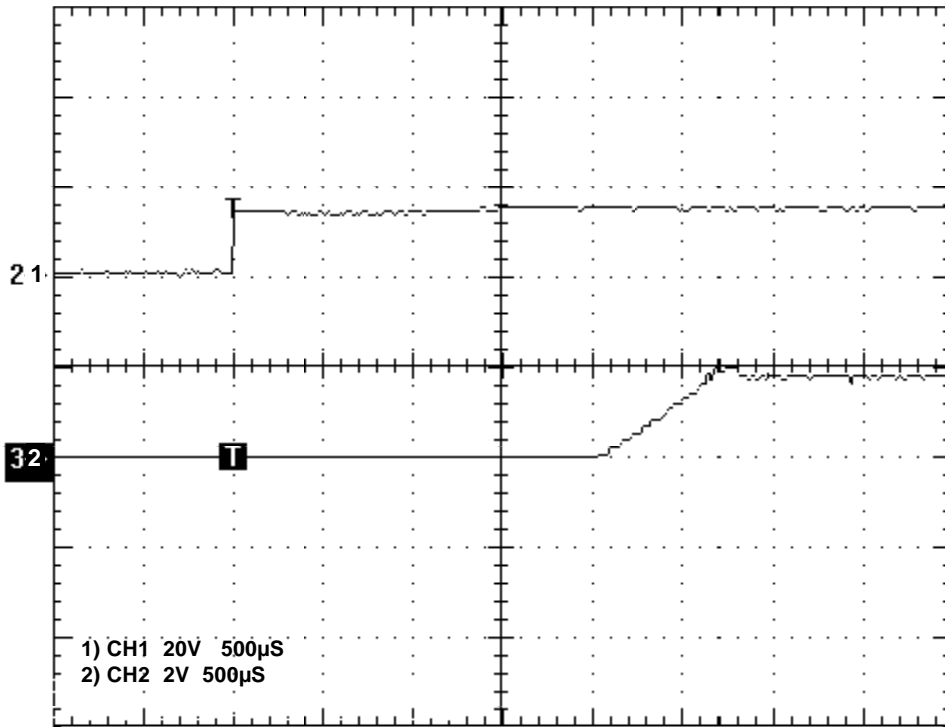


FIGURE 4. Turn on delay and soft start with 4700μF capacitor connected at the output

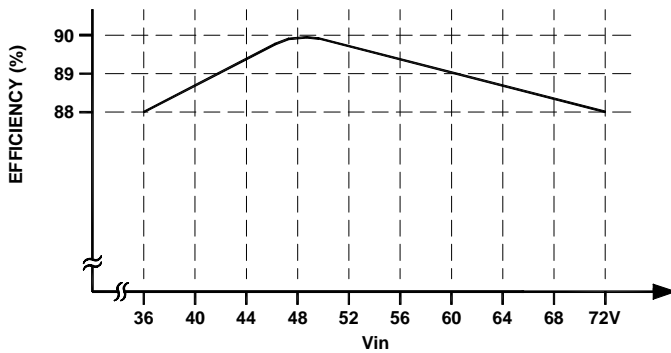


FIGURE 5A. Efficiency vs. Input Line for 3.3V_{OUT}

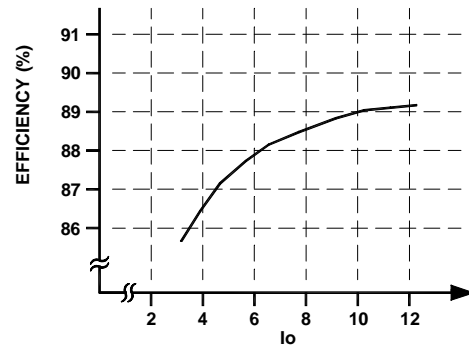


FIGURE 5B. Efficiency vs. Output Load for 3.3V_{OUT}

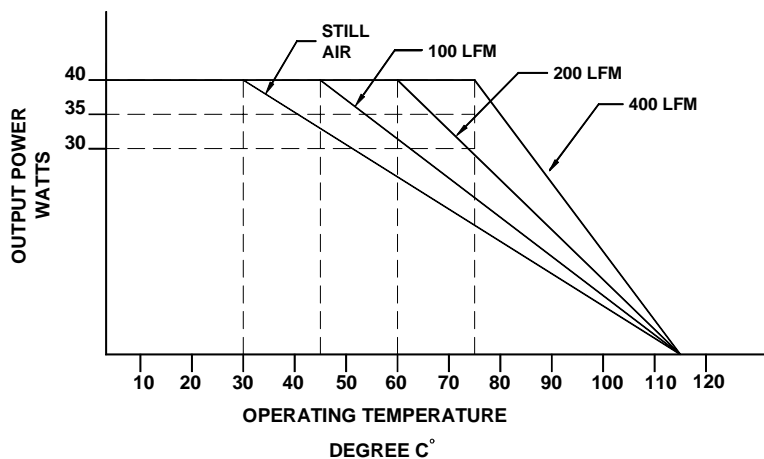
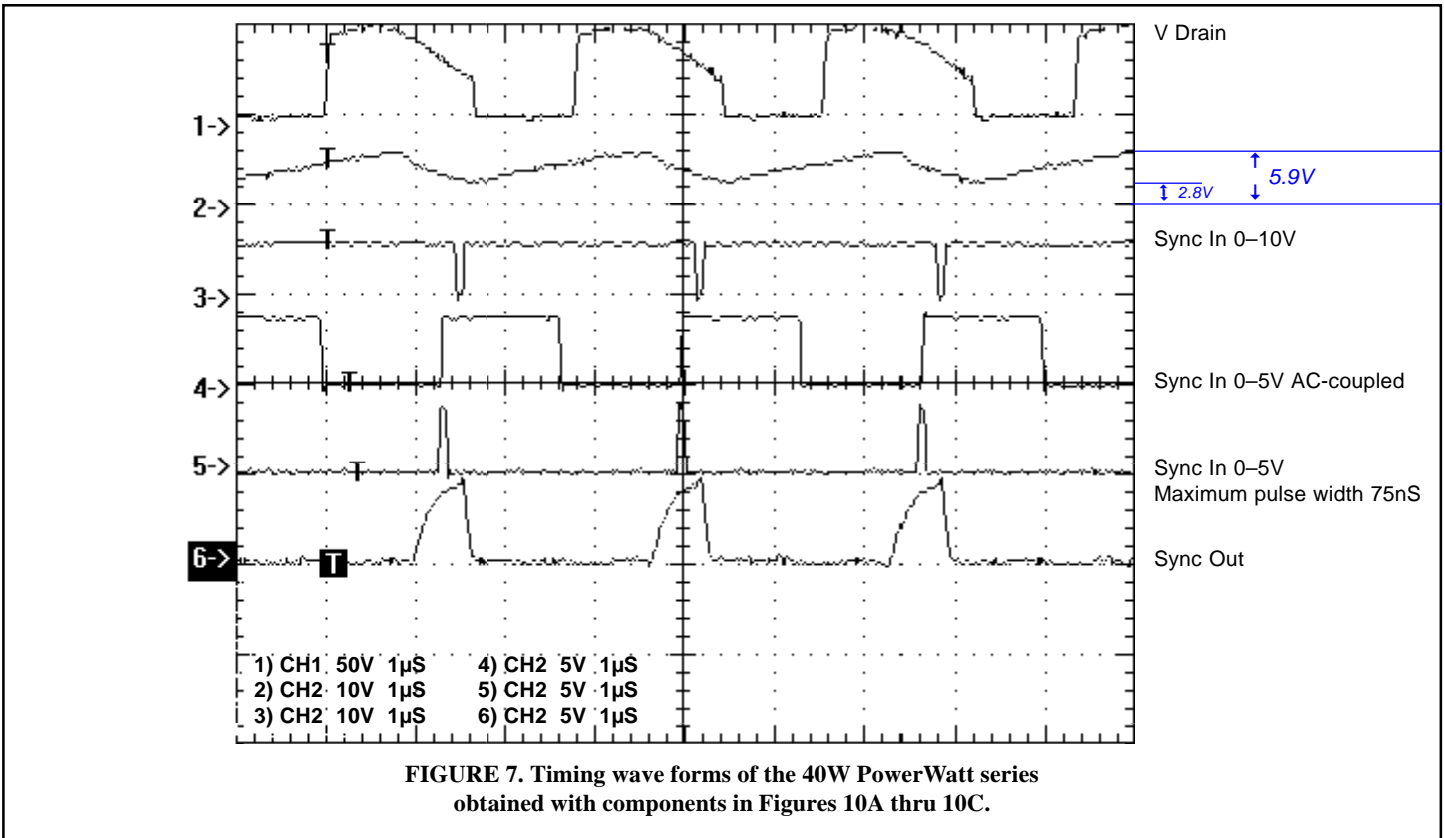


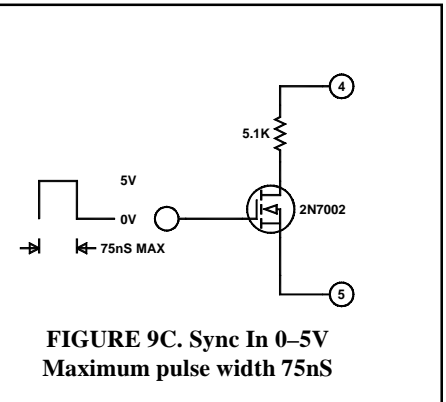
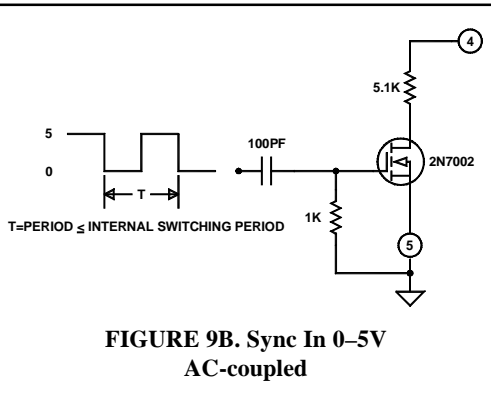
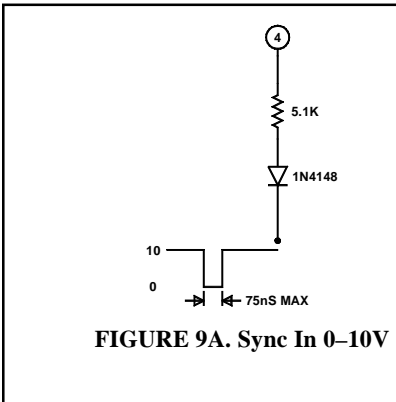
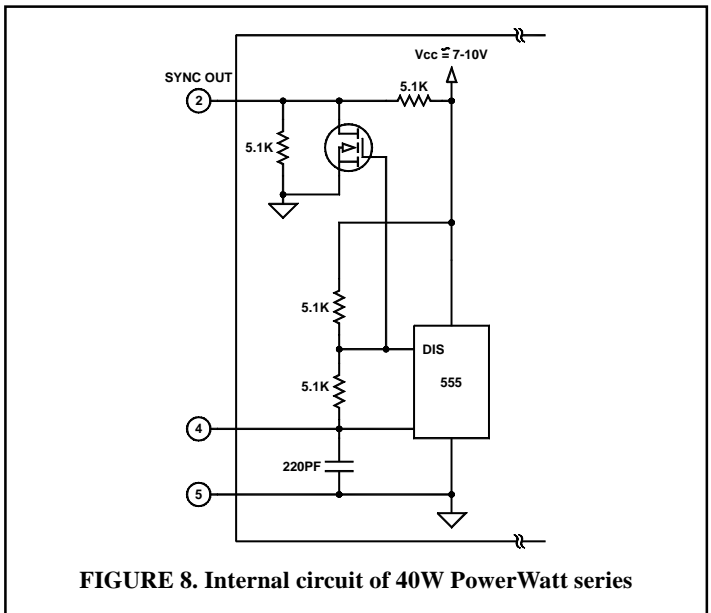
FIGURE 6. Worst case derating for 40W PowerWatt series



EXTERNAL SYNCHRONIZATION

The internal oscillator of the PWM is similar to that of a 555 timer (see Figure 8). The timing capacitor is connected to Pin 4 (Sync In), while the discharging node voltage of the oscillator is inverted and downconverted to provide the sync-out signal (Pin 2). The capacitor voltage of the oscillator varies between 1/3 of V_{CC} to 2/3 of V_{CC} . V_{CC} is the bias voltage to PWM and will vary from 7.5V under no load to approximately 10V under full load.

Figures 9A thru 9C shows three different ways of synchronizing the converter to an external clock. The external clock frequency **MUST** be less than or equal to the internal clock frequency. The 5.1kΩ resistor connected to Sync In (Pin 4) is used to prevent completely discharging the internal timing capacitor. Always place the 5.1kΩ as close as possible to Sync In (Pin 4) and avoid routing any other signal by this pin.



APPLICATION CONSIDERATIONS

Pin Functions

+V_{IN} (Pin 1): For positive input power supply connections.

SYNC OUT (Pin 2): Output-driving signal of the PWM; 0V to 6V.

ON/OFF (Pin 3): Turns converter off when pulled to ground through an open collector or open drain transistor. Maximum voltage at this pin is 10V minus a diode drop. Can be parallel connected with the ON/OFF pins of multiple converters or any Beta Dyne converter that may reside in the system. Leave this pin open for continuous operation.

SYNC IN (Pin 4): Input synchronization signal to the PWM. Used to synchronize the converter to an external frequency source. See **External Synchronization**.

-V_{IN} (Pin 5): For negative input power supply connection (or input ground).

-V_{OUT} (Pin 6): Negative output (GND).

-S (Pin 7): Negative output voltage sense; to be connected to the negative output.

V_{ADJ} (Pin 8): Output voltage adjust; to be used for an output voltage adjustment. Bypass this pin with a 0.01 μ F to 0.10 μ F capacitor. (Internal OPAM reference is connected to -V_{OUT}.)

+S (Pin 9): Positive output voltage sense; to be connected to the positive output voltage.

+V_{OUT} (Pin 10): Positive output voltage.

DESIGN CONSIDERATIONS

Input Source Impedance

The input of the converter should be connected to a low AC-impedance source. To reduce the impedance of a potentially high-inductive DC source, use a low ESR electrolytic capacitor (ESR < 0.6W@400kHz) mounted as close to the input pins as possible to ensure stability of the converter. As suggested in Figures 1 through 3, an electrolytic capacitor (22 μ F for 48V_{IN} or 47 μ F to 100 μ F for 24V_{IN}) in parallel with an SMD 2.2 μ F ceramic capacitor will ensure stability under any line or load condition. The 330 μ F capacitor before the input inductor L1 will reduce both reflected ripple and any long wire impedance from the DC source.

Output Filter Impedance

The impedance of an output filter may also affect the stability of a converter when additional low-pass filters are used. If additional output ripple reduction is required, avoid installing series inductors at the output. Instead, try to maximize output capacitance. The inductor of the output copper strips and a 1000 μ F capacitor will be enough for most applications. Low ESR electrolytic or tantalum capacitors can be used for additional output ripple reduction in parallel with ceramic capacitors for high-frequency attenuation. We recommend Vishay Sprague 594D Solid Tantalum Chip Capacitors.

THERMAL CONSIDERATIONS

Under full load, the 40W PowerWatt converters dissipate between 4W to 8W of power (depending on the model). The generated heat is transferred to the ambient by air conduction. At room temperature without any air movement, the operating environment of the converter is higher than room temperature, 25°–50°C higher, due to the fact that air around the converter heats up.

To measure the actual operating environment of the converter in a still air environment, place a thermocoupler a half-inch above the top center of the converter. Perform the same temperature measurement in a forced air convection system and use those temperature values for your thermal calculations. Do not assume the temperature is constant throughout a forced air cooling sys-

tem! Surrounding components and the load can cause the converter to go to thermal shutdown.

The minimum junction temperature of all semiconductors is 150°C and the maximum operating temperature of the PCB is 150°C. When the temperature of the PCB reaches approximately 125°C, the converter will turn off. The thermal hysteresis of 20°–30°C will allow the converter to cool off and resume operation once it reaches approximately 95°C. If there is not enough air circulation due to air fan failure of the system or very high environmental temperatures, the converter will stay in this so-called “hiccup” (ON/OFF) thermal mode indefinitely.

EXTERNAL TRIMMING OF OUTPUT VOLTAGES

To trim the output voltage DOWN, connect a 1% 1/8W resistor between the + (plus) output and trim pin of the converter. To trim the output voltage UP, connect a 1% 1/8W resistor between the – (minus) output and trim pins of the converter. For UP/DOWN trimming capability, connect a 10k Ω potentiometer between the + and – output pins, with the wiper arm connected to the trim pin. The trim resistors/potentiometer can be

connected at the converter output pins or the load. However, if connected at the load, the resistance of the runs becomes part of the feedback network which improves load regulation. If the load is some distance from the converter, connect the trim resistors/potentiometer at the same point where the sense pins are connected and bypass the V_{ADJ} and sense pins with a 0.01 μ F to 0.10 μ F capacitor at the converter pins.

EFFICIENCY MEASUREMENTS

Using the setup given in Figure 2, measure the input and output voltage at the pins at the top of the multiplayer PCB and

use these values to calculate the efficiency (see **Layout Considerations** for more details).

SHORT CIRCUIT PROTECTION

The PowerWatt series is designed to be a building block for higher power generation and to be able to charge very high output capacitance (up to 10,000 μ F). The internal current mode PWM is designed for power limit and it will not go into hiccup mode or latch off

when its output short circuits. When a short circuit is applied at the output of the converter, the PWM limits the input current to $I_{IN\ Max} + 25\%$ until thermal protection turns off the converter and forces it into thermal hiccup mode (see **Thermal Considerations**).

LAYOUT CONSIDERATIONS

The maximum output current of the converter is 18A and is carried to the load through 20A rated pins. When the converter is installed in a double-sided PCB, use both sides to connect the high current pins and use 2–3oz. copper for the plated through holes and/or power pads.

DO NOT USE sockets in production. For lab testing we recommend 3M/Textool ZIF sockets (P/N: 210-2599-000-0602) or any other socket that offers a maximum conductive surface to the pins.

If possible, maximize the surface area on the board for the power pins and DO NOT install a solder mask (see Figure 10). A solder mask will trap the heat inside the PCB and will not allow for maximum heat transfer even in forced-air cooling systems.

Please note that in a multilayer PCB the inner layers do not contribute much in reducing the thermal resistance of the power component, they only reduce the resistance to the load. If the top and bottom layers of your PCB can be plated up to 3–4 oz., you do not have to use a multilayer PCB for the converter.

If the sense run length exceeds 2 inches, the sense pins may have to be bypassed at a point close to the converter. Keep in mind to bypass to their respective polarity. Avoid running digital signal lines parallel to the sense or input sync pins. If more than one power device or converter is used per system board, use a star ground connection for all power devices.

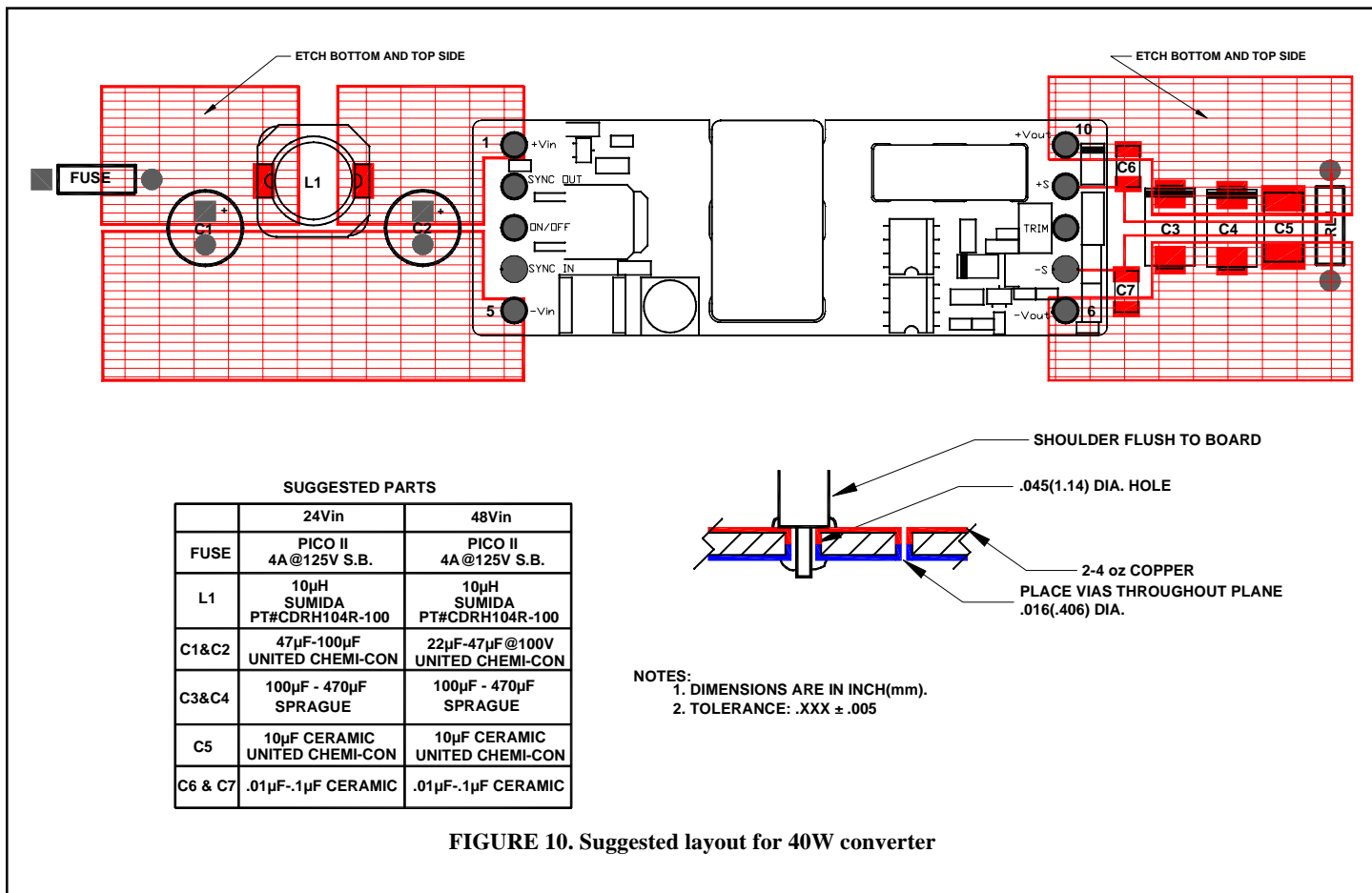
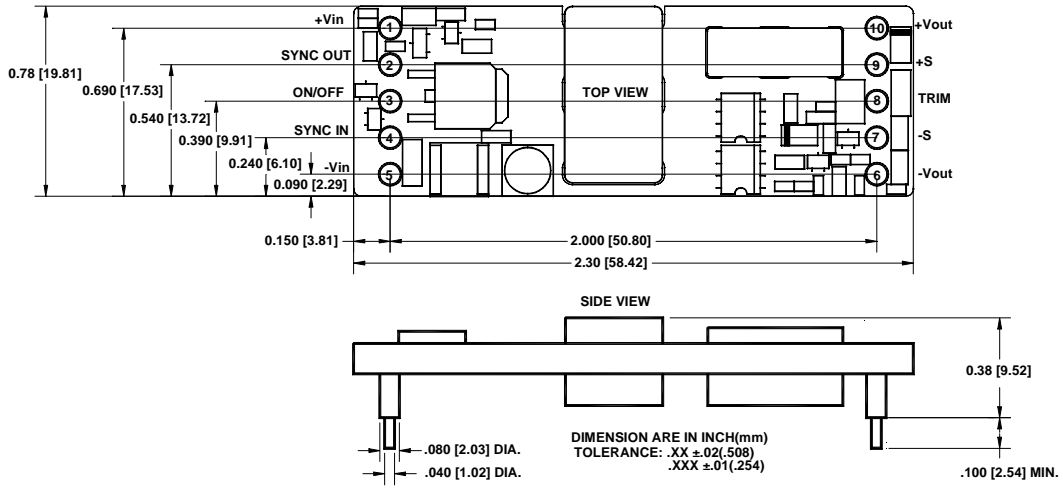


FIGURE 10. Suggested layout for 40W converter

MECHANICAL SPECIFICATIONS



Pin	Function
INPUTS	
1	+V _{IN}
2	SYNC OUT*
3	ON/OFF
4	SYNC IN*
5	-V _{IN}
OUTPUTS	
6	-V _{OUT}
7	-S
8	V _{ADJ}
9	+S
10	+V _{OUT}

* Optional pins,
 See Ordering Guide

EMI/RFI IN OPEN-FRAME DC/DC CONVERTERS

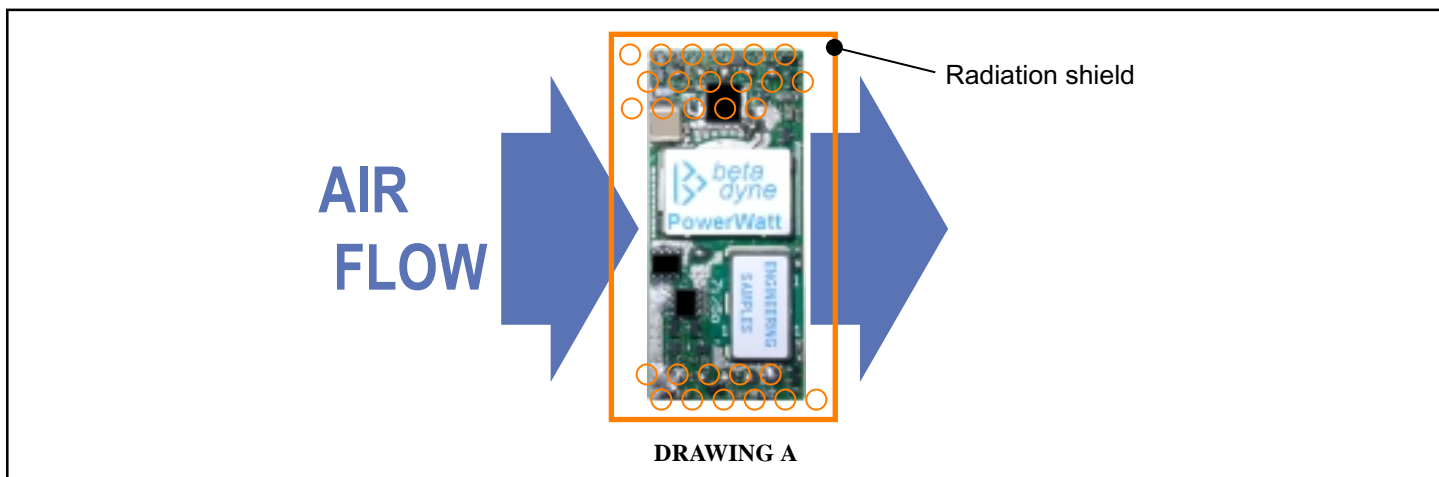
All switching AC/DC and DC/DC converters generate noise due to high-voltage, high-current internal switching. Conducted noise is the noise that appears at the point of conduct (pins) of the converter. Radiated noise is the electromagnetic noise transmitted to the environment from the power source. Conducted noise can be reduced to acceptable levels by an input/output low-pass filter.

In the past, manufacturers used metal cases and conductive headers to provide six-sided shielding to prevent radiated noise. Open-frame converters, on the other hand, have no shield and all the high-voltage, high-current switching points radiate noise. Open-frame, high-density DC/DC converters use forced air cooling. Most of the switching transistors are placed at the top of the converter to allow for better air circulation. Also, these switching transistors and power magnetics will produce square current/voltage waveforms that are full of harmonics. Most open-frame converters use fixed switching frequencies from 200kHz to 1MHz. The high switching frequencies can generate harmonics from 1MHz up to several hundred MHz.

The shield must allow the forced air to pass freely over the converter (see Drawings A, B & C). A metal screen can be considered. The holes in the screen must be less than the wavelength of the noise. If the converter is placed far from the load, make sure thick PCB runs are used (2–3 oz. copper is sufficient.)

When noise creates problems in a system, it is very difficult to identify the source of the problem. A poor layout with ground loop can not only create noise it can also affect the stability of the converter or randomly trigger an event. A common problem in high frequency and high power density DC/DC converters is the so-called “common-mode noise,” which is the noise generated from parasitic capacitors, leakage inductance, etc. in the converter.

Common-mode noise (CMN) can be bypassed to chassis with small capacitors between input and output grounds to chassis and input and output ground. Assuming the layout is correct and the converter still generates noise, the question then becomes why does the system not exhibit a noise problem when a linear



Effective placement and orientation of the converter in a system with forced air cooling can reduce the case temperature by 5–15°C (depending on the air flow (LFM)). When the converter is placed at the entrance and air passes over it as shown in Drawing A—from Pin 5–1 and 6–10—the lowest case temperature can be obtained.

Therefore, open-frame converters require special consideration in three critical areas—layout, radiation and cooling—that may create conflicts. We stress the importance of these critical areas:

LAYOUT RADIATION COOLING

When an open-frame converter is used to power digital circuits, radiation shielding can be implemented via the system shielding. When the load is an analog circuit—for example, A/D, D/A, RF amplifier, etc.—and these components are placed close to the converter, the radiated noise may affect signal integrity.

High impedance summing points of operational amplifiers or other components with poor power supply rejection ratio (PSRR) may be affected. In this case, local radiation shielding around the converter is necessary.

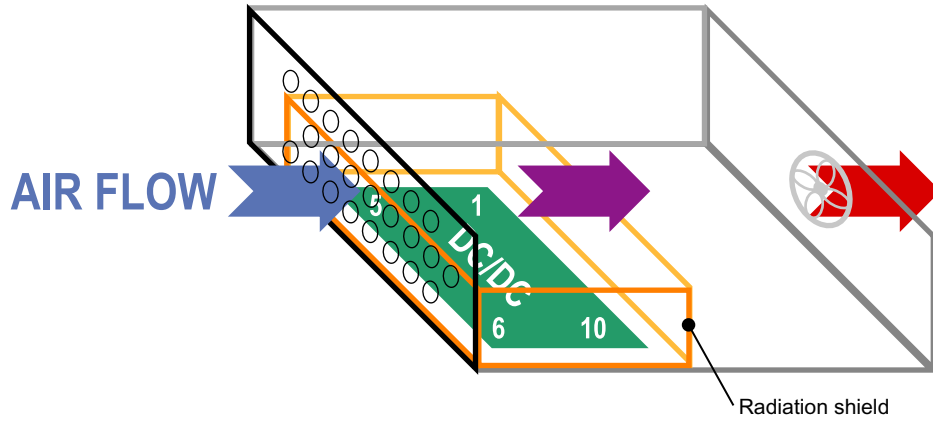
voltage source is supplied?

The answer comes from the process of elimination. Replacing a switching power source of 500kHz with another one switching at 50–60Hz is not the solution. Using the “noisy” DC/DC converter, one may try the following: First, if possible, shield the converter with six-sided shielding. If the problem is still in the system, then radiated noise is not the problem! Conducted noise or poor layout are the more likely causes. As was mentioned earlier, the use of a component with poor PSRR—e.g. BICMOS, CMOS, rail-to-rail OPAMS—may be the cause of the problem.

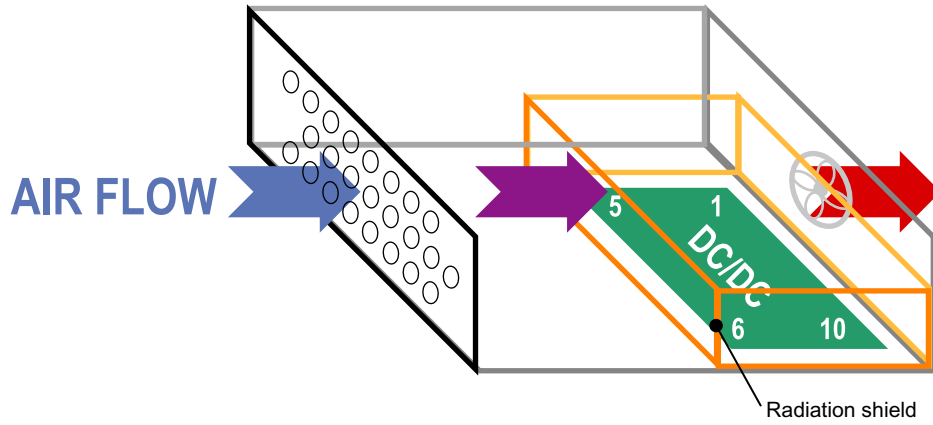
Do not use a converter with 50mV to 100mV output ripple to power a 12-bit A/D converter. Also keep in mind that CMOS, OPAMS, A/D, and S/H may offer low power, but the parasitic capacitor from drain to gate, drain to source, and gate to source will couple any V_{DD} and V_{SS} supply noise into your signal.

Better filtering in the input or output will reduce conducted noise if they are the cause of the problem. When both radiated and conducted noise are reduced, the last potential cause is **layout**. Also, use ground plain under the converter for shielding and avoid passing signal lines under it.

In conclusion, open-frame DC/DC converters offer high efficiency, power density, and low cost, but radiate a wide band of noise. For any application where the system layout is critical, select the appropriate converter(s) for the application and completely test your system during the prototyping phase. DO NOT ASSUME all is well. If your prototype function is worth it, do a complete evaluation.



DRAWING B



DRAWING C