Step-up Switching Regulators

STEP-UP (BOOST) NON-ISOLATED DC/DC CONVERTERS – THEORY OF OPERATION

When a low DC voltage source is used to power circuitry operating at high voltage levels, a step-up (boost) converter can be used. The input (lower voltage) is utilized to charge a passive component, such as a capacitor or inductor by the switching action of a transistor(s). Energy is stored in the passive component during the first charging phase of the operation and is delivered to the output on the second “discharging phase.”

In a low-power (less than 3W) boost converter, switching capacitors are used. They offer small size and efficiencies up to 97% when the switching is implemented through low RDS_{ON} MOSFETs. Depending on the number of switched capacitors used, the maximum V_O is given by:

$V_O \leq V_{IN}(1+N)$, where N = number of capacitors.

For higher power and output voltage, an inductor is used for energy storage transfer as shown in Figure 1. When Q_1 is off, **$V_O = V_1 - V_{D1}$**.

The pulse width modulator (PWM), through a negative feedback loop, controls the duty cycle of Q_1 and thus regulates V_O. When Q_1 turns on, D_1 disconnects V_O (D_1 is reversed bias and C_O provides all the power to the load during this phase). A current starts to flow through L_1, Q_1 to the ground magnetizing L_1.

Energy stored in the magnetic field of an inductor is given by:

$$\mathbf{E(t) = 0.5L(I(t))^2 \Leftrightarrow (E \text{ in a cap is } E(t) = 0.5C(V(t))^2)}$$

After a time period, Q_1 turns off, the current through the inductor drops to zero and causes the magnetic field to reverse and a high voltage appears at the inductor–transistor–diode node A. When $V_A = V_O + V_D$ (where V_A is the voltage at node A), the energy that was stored in L is transferred to the output through D_1 and charges C_O back to V_O Nominal. When V_O drops a few mV below V_O Nominal, the PWM turns on Q_1 and the process repeats.

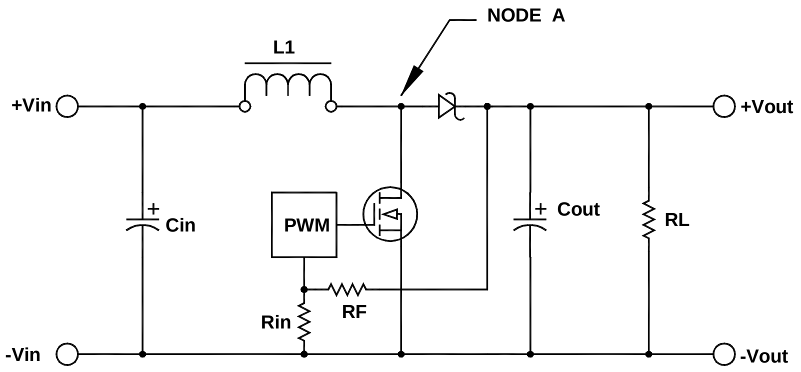


FIGURE 1. Step-up switching regulator

To better understand the two-phase operation of the boost converter, the schematic in Figure 1 is separated into two sections. Figure 2A shows the charging phase operation and Figure 2B displays the discharging phase operation. NOTE: the charging/discharging phase is used with respect to the energy storing and transferring element in the circuit, which in our case is L_1.

In Figure 2A, Q_1 is on and it is replaced by its RDS_{ON} at t0 (see Figure 3), and L_1 is magnetized by I_1 and I_2. Resistor R_S is the sum of the internal source resistance and any wire or PCB trace resistance from V_{IN} to L_1. Resistor ESR is the equivalent series resistance of the input capacitor C1. During the inductor charging phase to t1, the power dissipated in the circuit in Figure 2A is given by:

$$P_D = I^2R_S + I^2ESR + I^3RDS_{ON}$$

where it is assumed L1 has no drops.

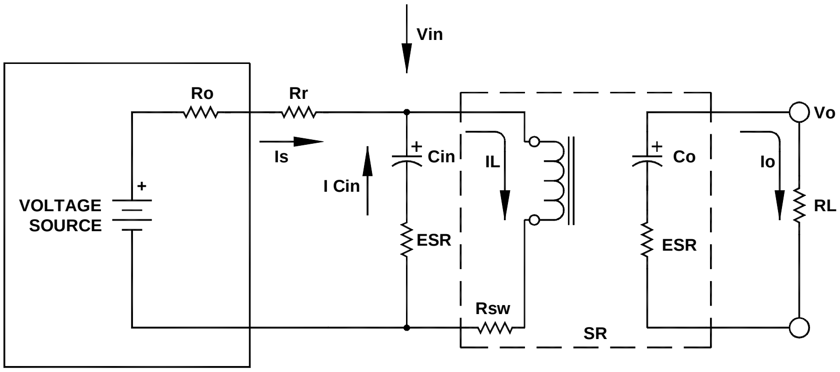
In order to minimize the power dissipation in this circuit, it is obvious that all resistance must be as low as possible; C_{IN} must have the lowest ESR and high current ripple rating. The source resistance can be reduced if high-gauge wire or thick PCB traces are used. But if the source resistance of V_{IN} is high, such as different batteries or unregulated power supplies, C_{IN} is forced to supply most of the required energy for L_1. When $I_2 > I_1$, the power dissipated in C_{IN} can cause C_{IN} to overheat and eventually short circuit the input.

Many times the question is asked, “Why doesn’t the converter work at minimum V_{IN}?” If the input voltage drops momentarily below the undervoltage protection threshold of the converter, the converter will go to shutdown momentarily and “will not work.” To verify that a given converter “does not work,” use an oscilloscope and *not* a voltmeter.

At t1, Q1 turns off the voltage at node A in Figure 1. Node A then becomes much higher than V_{IN} and when $VA > V_O + V_{D1}$, the energy stored in L1 during the charging phase (t0 to t1) is transferred (discharged) to the output from t1 to t2 (see Figure 3). The equivalent circuit for the discharge phase is given in Figure 2B. The inductor, L_1, is shown as a current source, I, passing through D_1, recharging C_O, and supplying the I_{RL} for the load.

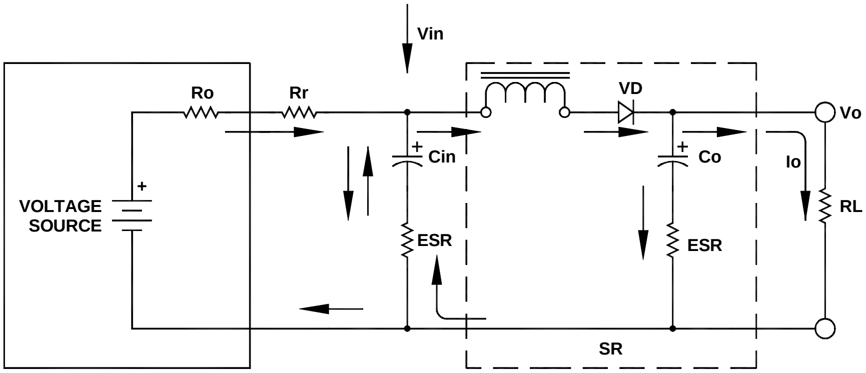
The power dissipation in the converter during the discharge phase is given by:

$$P_D = I^2ESR_{Cin} + V_{DI} + (I_{Co})^2ESR_{Co}$$



Equivalent Circuit for t0 ≤ t ≤ t1
I3 = I1 + 12

FIGURE 2A. Charging phase



Equivalent Circuit for t1 ≤ t ≤ t2
$I = I\ C_{OUT} + I\ RL$

FIGURE 2B. Discharging phase

If the ESR of both capacitors C_{IN}, C_O are minimized, the only remaining power-dissipating component is the diode D_1. In synchronous rectifying step-up converters, the diode D_1 is replaced with a MOSFET in order to reduce the power dissipation (see Figure 4).

The effects of low and high ESR can be seen in Figure 3, traces 2 and 6 (B, F) respectively. For C_O, a 200µF 100V aluminum electrolytic capacitor with long lead was used in purpose and without snubbers.

In Figure 4, a step-up converter with synchronous rectification is given. The circuit operates the same as the circuit in Figure 1. The MOSFET Q_2 is used in order to reduce the power dissipation in D_1. The converter in Figure 4 is more expensive, requires more parts and may not provide better efficiency. The timing for the switching of Q_1, Q_2 is critical; Q_2 must turn on when its source voltage becomes equal or greater than V_O.

On the other hand, if Q_2 turns on a few nanoseconds after its source voltage equals V_O, the parasitic diode of Q_2 will be forced on causing even higher $V_D \times I$ drops due to the fact that the forward drop of the parasitic diode is much higher than that of a Schottky diode. To prevent the parasitic diode from turning on, a Schottky diode is placed between source and drain of Q_2 as shown in Figure 4. The parasitic capacitors of Q_2 such as gate-to-source, gate-to-drain, and drain-to-source will also contribute to the power dissipation. The power dissipation in a capacitor is given by:

$$P = 2*E*F$$

where $E = \frac{1}{2}CV^2$, F = switching frequency, and V = the applied voltage across each capacitor.

It should be noted that C_{DS} switches between V_O and ground, C_{GD} from V_O to V_{GATE}. When the cost versus benefit is considered, a 1–2% increase in efficiency with a synchronous rectifying converter may not be worth it.

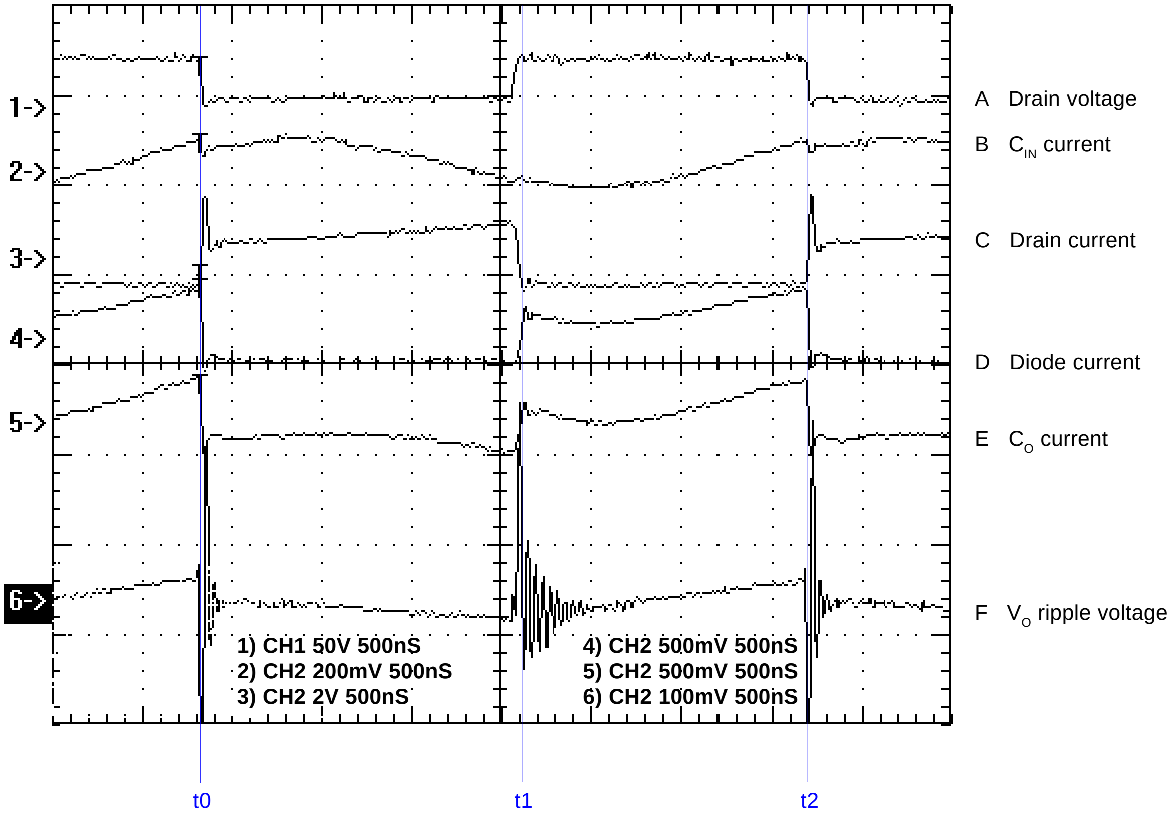


FIGURE 3. Typical waveforms of step-up switching regulators

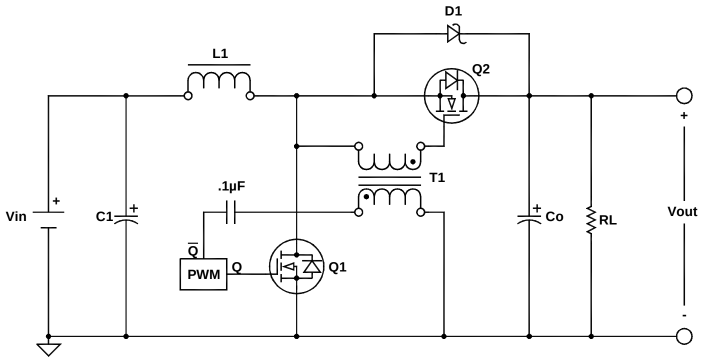


FIGURE 4. Synchronous step-up switching regulator

SHORT CIRCUIT PROTECTION

Referring to Figures 1 and 4, it is obvious that step-up converters have no output short circuit protection. A direct current path exists from +V_{IN} to +V_{OUT} through L_1 and D_1. An input fuse can be used between V_{IN} and C_{IN} as shown in Figure 5. The current rating must be higher than the maximum input current, which would also result in an increase in power dissipation (R Fuse*I_{IN}^2) and a forcing of higher current through C_{IN}.

If short circuit protection is absolutely necessary, one may try the circuit given in Figure 6. A high current transistor Q_1 is used as an on/off switch and the input current sensing is accomplished by I_{C1}. I_{C1} is a current sense amplifier with three different current gains: 20, 50, and 100 V/V. The output of I_{C1} (Pin 2) is proportional to I_{IN}. Therefore, the output of the IC must be delayed turning the turn on to allow I_{IN} to charge the input capacitance and the DC/DC converter must have a soft-start feature to slowly charge the output capacitors.

The turn on delay can be adjusted with R_2, C_2. The off time of Q_1 is also adjustable through D_1, C_3, R_3. When V_O of I_{C1} reaches the threshold of Q_2, the gate of Q_1 is pulled low and the converter is disconnected from the input supply. When capacitor C_4 is installed, it can reduce the inrush current I_{IN} at turn on and thus will allow the converter to be “hot pluggable.” The output of I_{C1} can also be used for I_{IN} monitoring by a CPU if it is converted to a digital form by an A/D converter.

In conclusion, step-up converters offer high efficiency, low cost, and high operating life. They are P.O.L. converters and when the designer observes the manufacturer’s application guidelines, they will perform.

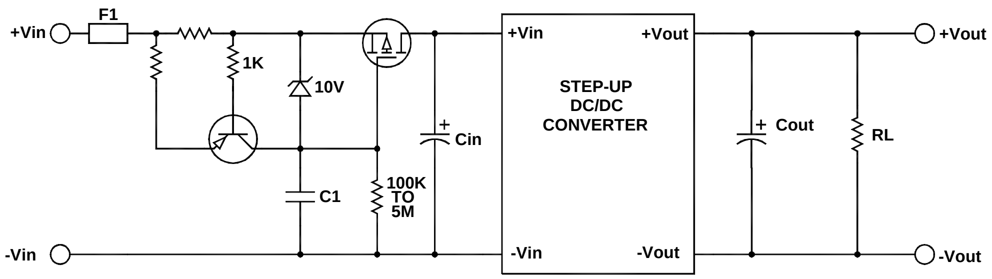


FIGURE 5. Short circuit protection for low-power converters

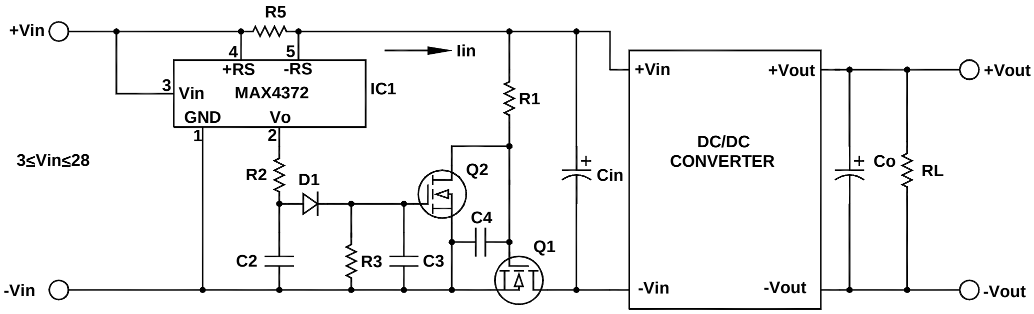


FIGURE 6. Short circuit protection with hot pluggability