

SR50

50W SWITCHING REGULATOR
 15A Output Current, Multi-modes of Operation
 Six Different VID Codes

Standard Features

- Synchronizable fixed frequency
- Over/under input voltage protection
- Wide V_{IN} range: 2.5V to 12V operation
- 5-bit digital-to-analog V_{OUT} selection:
 - 0.925V to 2.00V range with 50mV/25mV steps
 - 1.3V to 3.5V range with 100mV/50mV steps
 - 1.65V to 5V range with 150mV/75mV steps
- $\pm 1\%$ output voltage accuracy
- Power good output voltage monitor
- Output overvoltage crowbar protection
- Internal current foldback
- Internal overvoltage protection
- Soft start
- Remote output voltage sense
- Industry standard pinout
- Thermal protection

Optional Features

- A: Active Voltage Positioning
- B: Latched Short Circuit
- C: Skip Mode Operation
- D: Single Wire Output Current Share



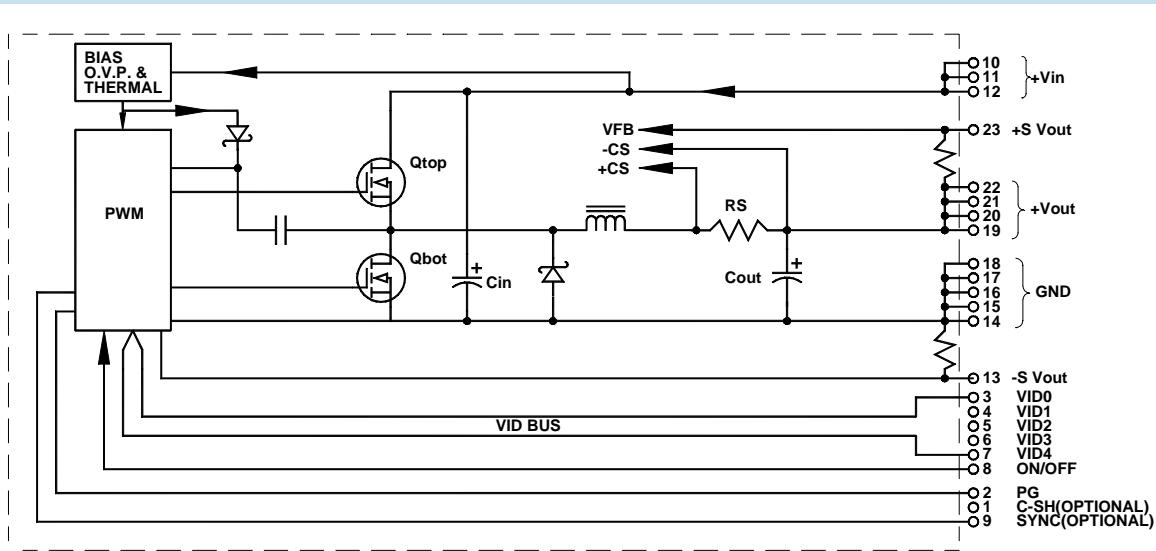
Applications

- Desktop Computers
- Notebook and Palmtop Computers
- Personal Digital Assistants (PDA)
- Mobile Intel® Pentium® II and III CPUs
- Low-Voltage Adjustable Power Supplies
- Reference Supplies for DDR SDRAM

Functional Description

The SR50 is a family of 5-bit, adjustable, synchronous, non-isolated step-down switching regulators designed for CPU power. The SR50 offers a high degree of customizability with its support for a wide range of input and output voltages, six different VID codes, choice of two physical configurations, and substantial optional feature set. The input voltage range of these converters is from 3.3V to 12V with standard inputs of 3.3, 5, and 12V. The 5-bit DAC programs the output voltage required

by most VRM converters specified by CPU manufacturers. The output can be programmed by the VID codes to conform to VRM 8.1 to 8.4 output voltage or be set to any other customer-specified programmable output within 0.9V to 5V. The standard output VID programmable range is 0.9–2V, 1.3–3.5V, and 1.7–5V. The synchronous rectifiers operate at 400kHz switching frequency, which can be synchronized to an external clock. The multilayer PCB minimizes thermal resistance.



Typical Block Diagram

Electrical Specifications

Unless otherwise specified, all parameters are given under typical +25°C with nominal input voltage and under full output load conditions.

INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Input Voltage Range	See Model Selection Guide				
Input Current, No Load	See Model Selection Guide				
Input Current, Full Load	See Model Selection Guide				
Input Reflected Ripple	See Model Selection Guide				
Off State Input Current	See Model Selection Guide				
Remote On/Off Control	Reference to GND, Open = ON, Short = OFF				
Sync, Forced Continuous Threshold		0.76	0.8	0.84	Vdc
Sync, Forced Continuous Current	$V_{\text{SYNC}} = 0.85\text{V}$		-0.17	-0.3	μA
PGOOD Output					
PGOOD Voltage Low	$I_{\text{PGOOD}} = 2\text{mA}$		110	200	mV
PGOOD Leakage Current	$V_{\text{PGOOD}} = 5\text{V}$			± 1	μA
PGOOD Trip Level	V_{OSENSE} with Respect to Set Output Voltage				
	V_{OSENSE} Ramping Negative	-6.0	-7.5	-9.5	%
	V_{OSENSE} Ramping Positive	6.0	7.5	9.5	%
VID Control					
VID Operating Supply Voltage		2.7		5.5	Vdc
VID Supply Current			0.01	5	μA
VID0 to VID4 Pull-Up Resistance			40		$\text{k}\Omega$
VID Input Voltage Threshold		0.4	1.0	1.6	Vdc
VID Input Leakage Current	$\text{VIDV}_{\text{CC}} < \text{VID} < 7\text{V}$		0.01	± 1	μA
VID Pull-Up Voltage	$\text{VIDV}_{\text{CC}} = 3.3\text{V}$		2.8		Vdc
	$\text{VIDV}_{\text{CC}} = 5\text{V}$		4.5		Vdc
Turn On Delay	Including soft start		5		mS
Input Overvoltage Shutdown	See Model Selection Guide				

OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Output Voltage Range	See Model Selection Guide				
Line Regulation			± 0.2	± 0.5	%
Load Regulation			± 0.2	± 0.2	%
Ripple and Noise			25	50	mV
Temperature Coefficient			0.01		%
Transient Response	$V_{\text{IN}} = 5\text{V}$, NL to FL		10	20	μS
Thermal Shutdown	Case temperature	100	110	125	$^{\circ}\text{C}$
Recovery from Thermal Shutdown		80	85		$^{\circ}\text{C}$
Short Circuit Current			0.6		A
Overvoltage Lockout	$V_{\text{O}} > V_{\text{O}}$ Nominal		7.5		%

GENERAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Efficiency	See Model Selection Guide				
Switching Frequency	Fixed	360	380	400	Hz
External Clock Frequency Range		330		440	kHz
Isolation	None				
Thermal Resistance	Internally dissipated		0.3	0.4	$^{\circ}\text{C}/\text{W}$
MTBF	per MIL-HNBK-217F (Ground benign, +25°C)		984,000		hours

ENVIRONMENTAL / PHYSICAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Humidity	Non-condensing			95	%
Storage Temperature		-60		+125	$^{\circ}\text{C}$
Operating Temperature, Commercial		-40		+75	$^{\circ}\text{C}$
Operating Temperature, Extended		-55		+85	$^{\circ}\text{C}$
Dimensions, With Heat Sink (LxWxH)	2.60x1.10x0.52 in. (66.04x27.94x13.21mm)				
Weight, With Heat Sink	1.2 oz. (34g)				

TABLE 2. Voltage Identification Code [VID B]

					VID B	VID B'
VID4	VID3	VID2	VID1	VID0	V _{OUT} (V)	V _{OUT} (V)
0	1	1	1	1	1.30	2.00
0	1	1	1	0	1.35	2.10
0	1	1	0	1	1.40	2.20
0	1	1	0	0	1.45	2.30
0	1	0	1	1	1.50	2.40
0	1	0	1	0	1.55	2.50
0	1	0	0	1	1.60	2.60
0	1	0	0	0	1.65	2.70
0	0	1	1	1	1.70	2.80
0	0	1	1	0	1.75	2.90
0	0	1	0	1	1.80	3.00
0	0	1	0	0	1.85	3.10
0	0	0	1	1	1.90	3.20
0	0	0	1	0	1.95	3.30
0	0	0	0	1	2.00	3.40
0	0	0	0	0	2.05	3.50
1	1	1	1	1	2.00	1.30
1	1	1	1	0	2.10	1.35
1	1	1	0	1	2.20	1.40
1	1	1	0	0	2.30	1.45
1	1	0	1	1	2.40	1.50
1	1	0	1	0	2.50	1.55
1	1	0	0	1	2.60	1.60
1	1	0	0	0	2.70	1.65
1	0	1	1	1	2.80	1.70
1	0	1	1	0	2.90	1.75
1	0	1	0	1	3.00	1.80
1	0	1	0	0	3.10	1.85
0	0	0	1	1	3.20	1.90
1	0	0	1	0	3.30	1.95
1	0	0	0	1	3.40	2.00
1	0	0	0	0	3.50	2.05

NOTE: Table shows the full VID range for reference.

V_{OUT} requirements are:

- 1.8V-2.8V for Intel® Pentium® II processors
- 1.8V-2.05V for Intel® Pentium® II and Pentium® III processors
- 1.3V-2.05V for Intel® Celeron™ processors

TABLE 3. Voltage Identification Code [VID C]

					VID C	VID C'
VID4	VID3	VID2	VID1	VID0	V _{OUT} (V)	V _{OUT} (V)
0	1	1	1	1	1.650	2.700
0	1	1	1	0	1.725	2.850
0	1	1	0	1	1.800	3.000
0	1	1	0	0	1.875	3.150
0	1	0	1	1	1.950	3.300
0	1	0	1	0	2.025	3.450
0	1	0	0	1	2.100	3.600
0	1	0	0	0	2.175	3.750
0	0	1	1	1	2.250	3.900
0	0	1	1	0	2.325	4.050
0	0	1	0	1	2.400	4.200
0	0	1	0	0	2.475	4.350
0	0	0	1	1	2.550	4.500
0	0	0	1	0	2.625	4.650
0	0	0	0	1	2.700	4.825
0	0	0	0	0	2.775	5.000
1	1	1	1	1	2.700	1.650
1	1	1	1	0	2.850	1.725
1	1	1	0	1	3.000	1.800
1	1	1	0	0	3.150	1.875
1	1	0	1	1	3.300	1.950
1	1	0	1	0	3.450	2.025
1	1	0	0	1	3.600	2.100
1	1	0	0	0	3.750	2.175
1	0	1	1	1	3.900	2.250
1	0	1	1	0	4.050	2.325
1	0	1	0	1	4.200	2.400
1	0	1	0	0	4.350	2.475
1	0	0	1	1	4.500	2.550
1	0	0	1	0	4.650	2.625
1	0	0	0	1	4.825	2.700
1	0	0	0	0	5.000	2.775

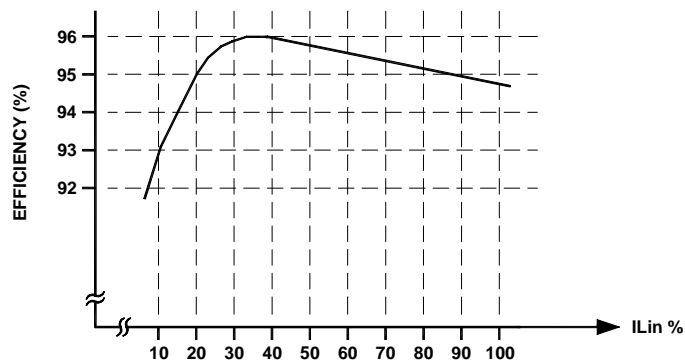


FIGURE 1. Efficiency vs. Load

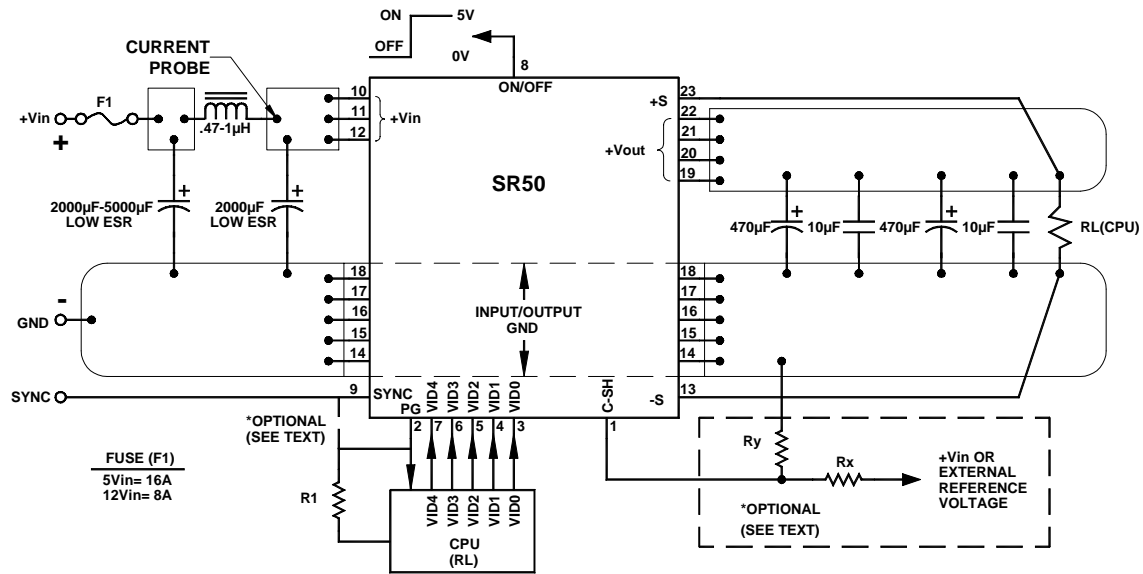


FIGURE 2A. Typical connection diagram
(See Figure 1B for more info)

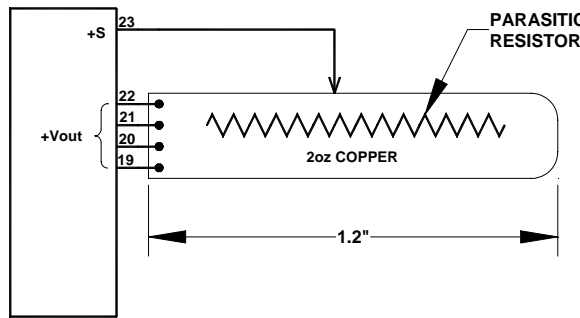


FIGURE 2B. Close-up view of output current limiting

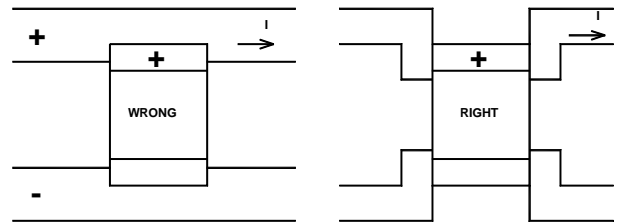


FIGURE 2C. Close-up view of output current limiting

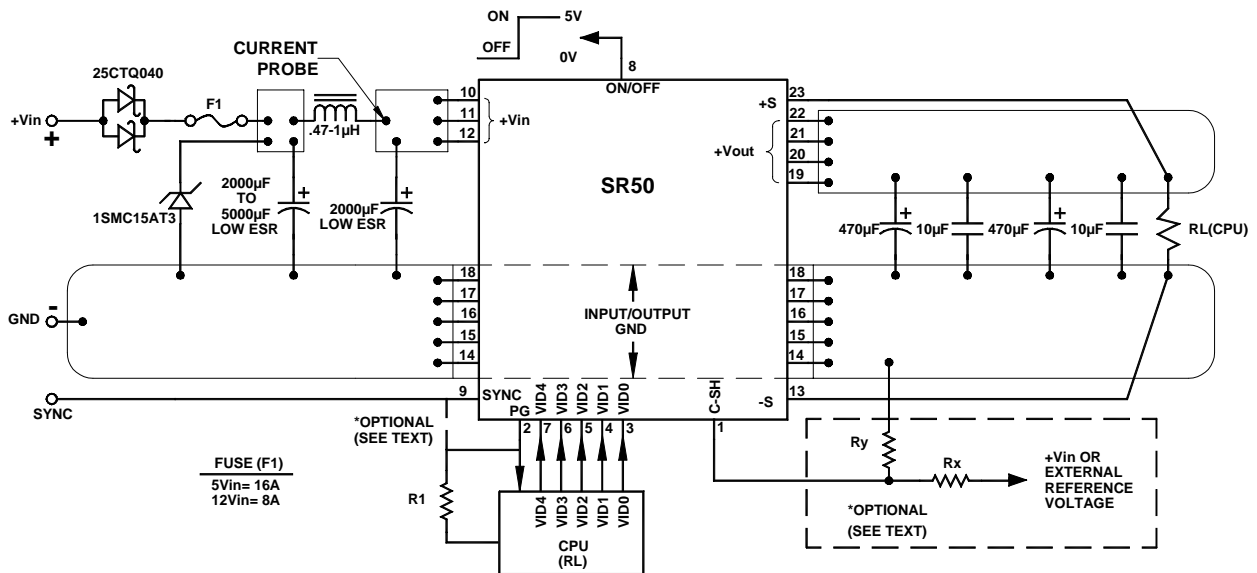
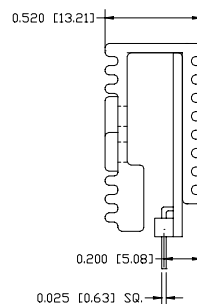
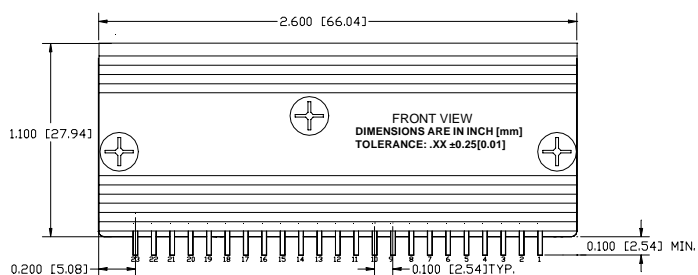
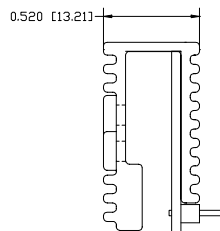
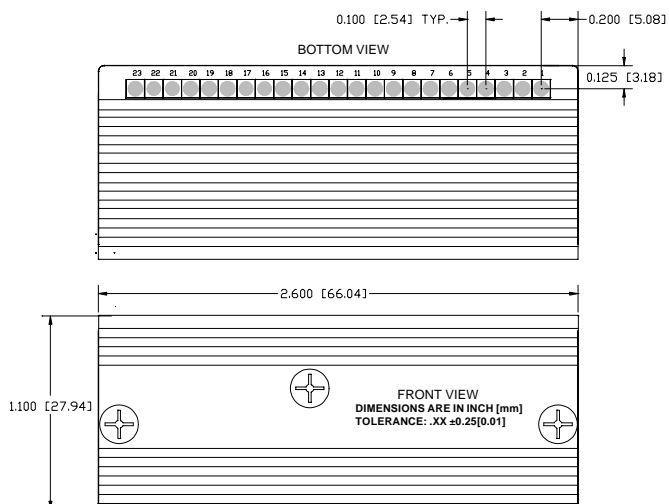
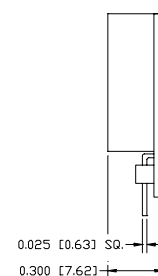
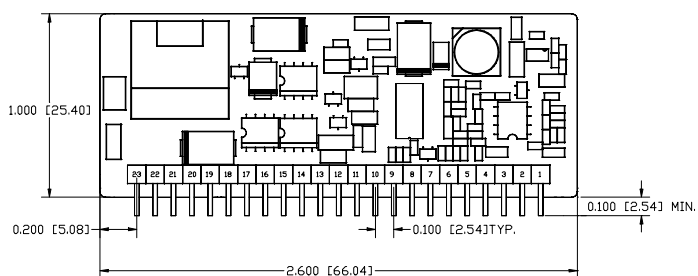
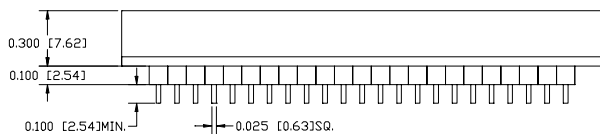
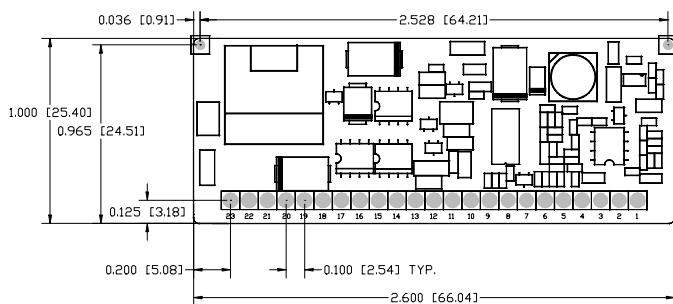


FIGURE 3. Typical connection diagram for automotive applications

MECHANICAL SPECIFICATIONS WITH HEAT SINK



WITHOUT HEAT SINK



Pin	Function
1	C-SH (Optional)
2	Power Good (PG)
3	VID0
4	VID1
5	VID2
6	VID3
7	VID4
8	ON/OFF
9	SYNC (Optional)
10	+V _{IN}
11	+V _{IN}
12	+V _{IN}
13	-S V _{OUT}
14	GND
15	GND
16	GND
17	GND
18	GND
19	+V _{OUT}
20	+V _{OUT}
21	+V _{OUT}
22	+V _{OUT}
23	+S V _{OUT}

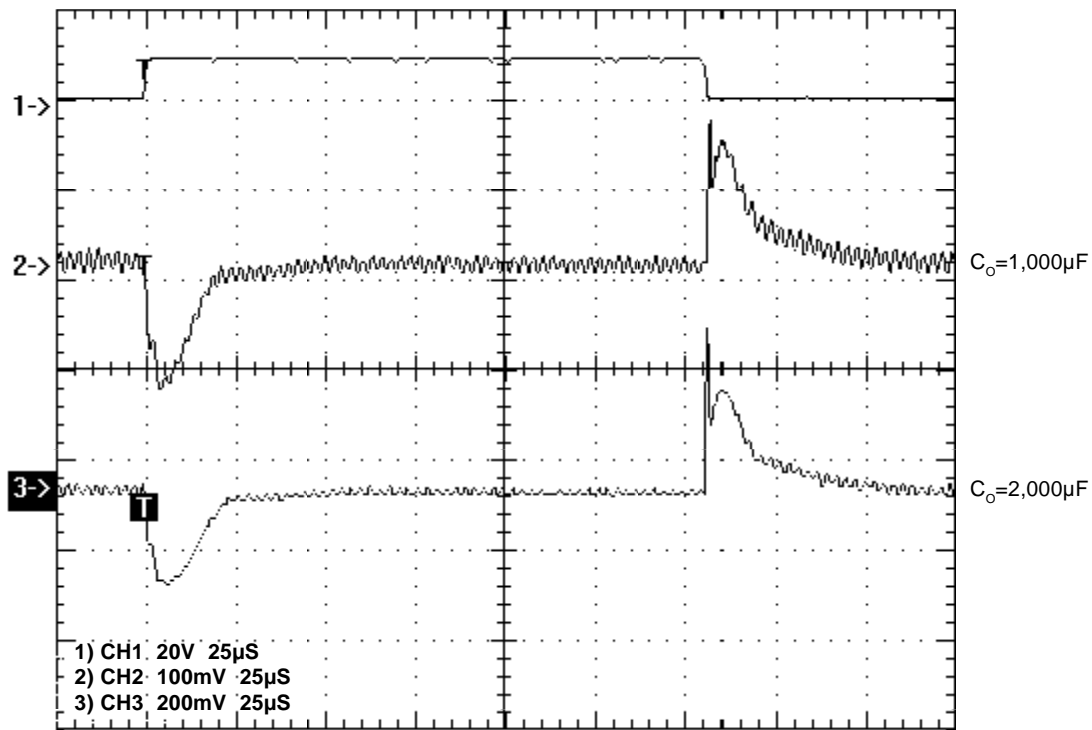


FIGURE 4. Transient response of SR50_1.3-3.5/5 at $V_o = 3.5\text{V}$
 50% FL to FL to 50% FL

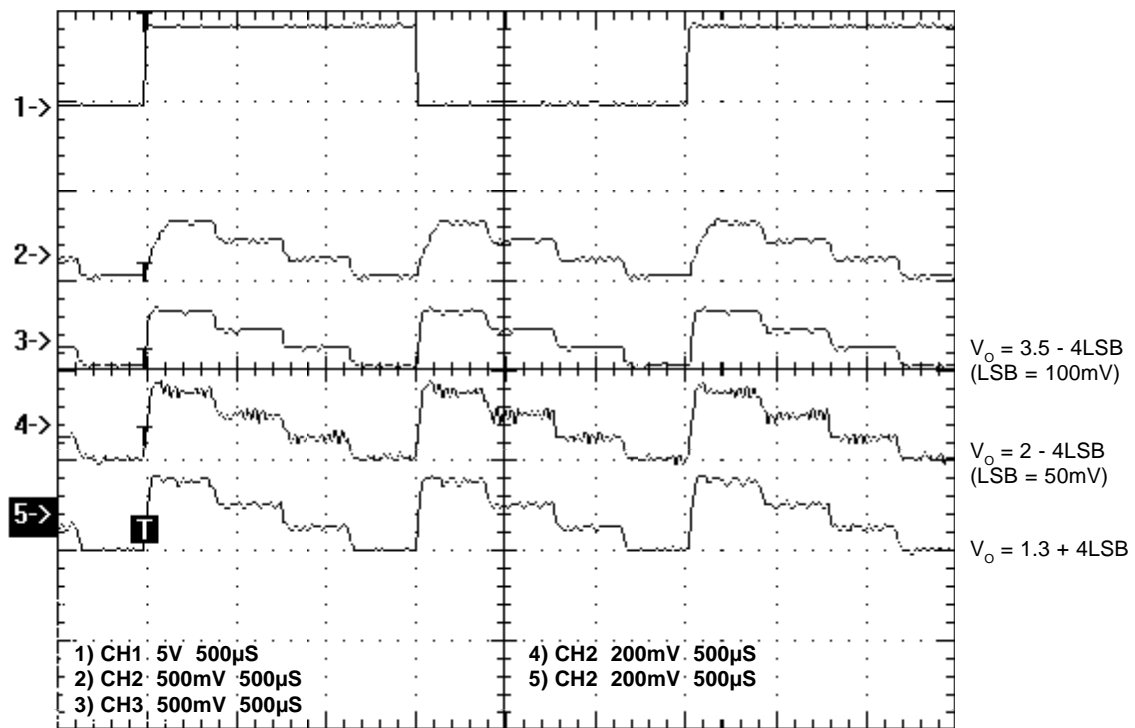


FIGURE 5. Output response of SR50_1.3-3.5/5 with VID switching

- 1) Sync signal
- 2) Effect of current limiting circuit when Power Run $> 0.003\Omega$
- 3) Effect of current limiting circuit when Power Run $\leq 0.003\Omega$
- 4 & 5) Dynamic switching at different output settings

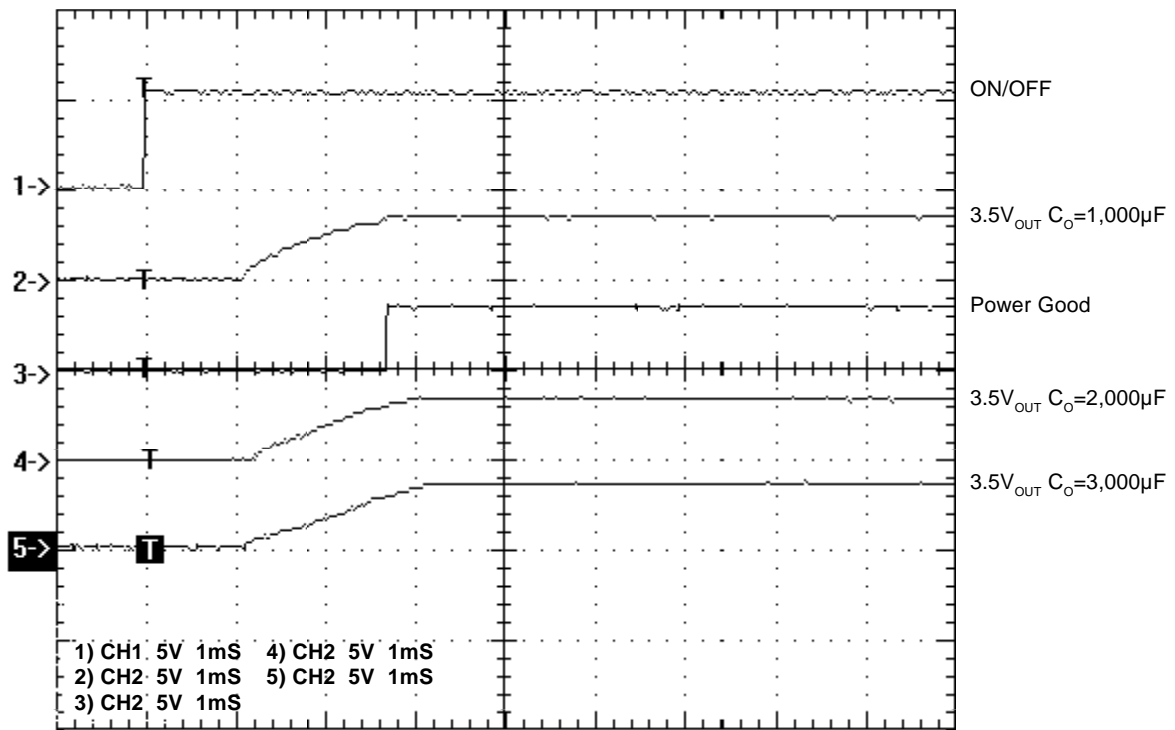


FIGURE 6. Turn on delay with soft start and power good with different capacitor loading, $I_o=15A$

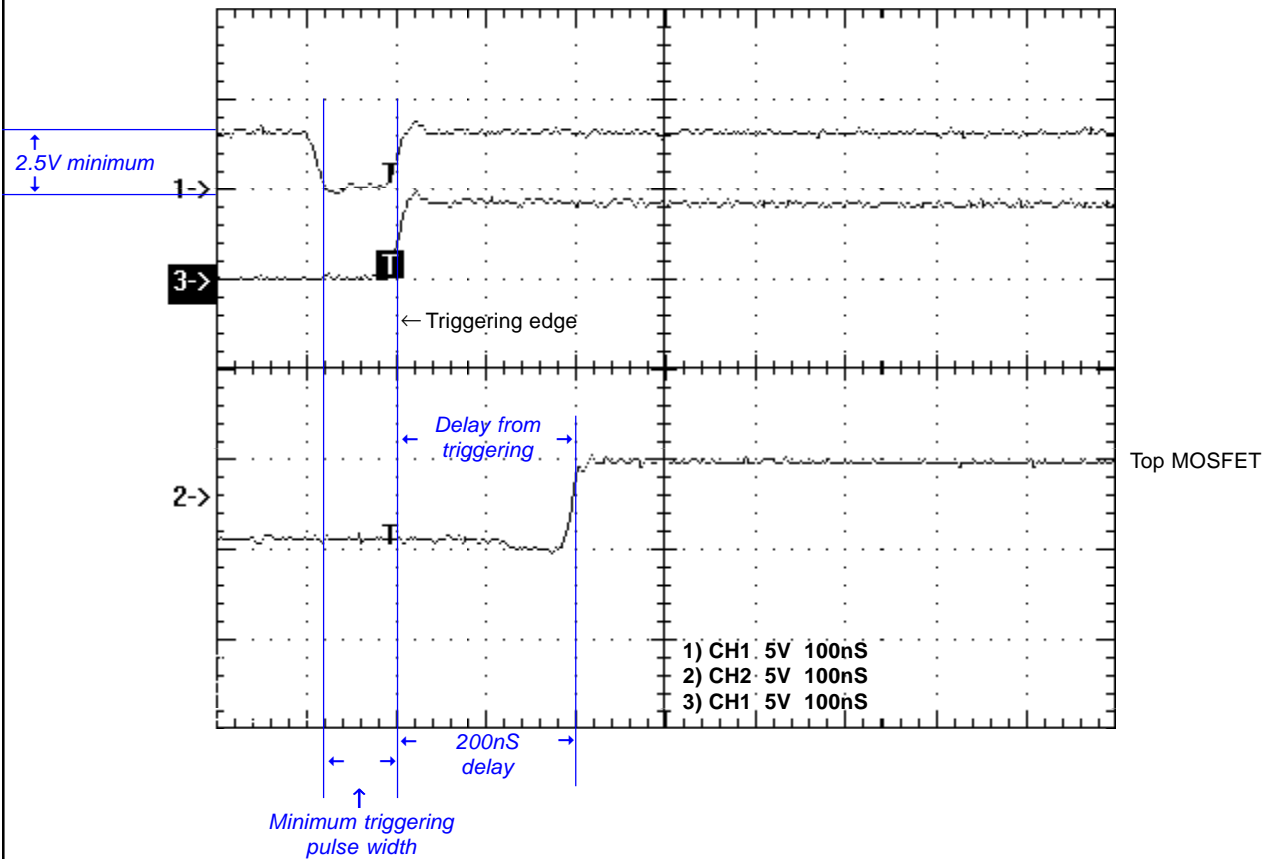


FIGURE 7. External sync waveforms

- 1) Minimum pulse with clock in signal
- 2) Positive edge initiates synchronization
- 3) Time delay from the positive edge of the external clock to the beginning of synchronous rectification

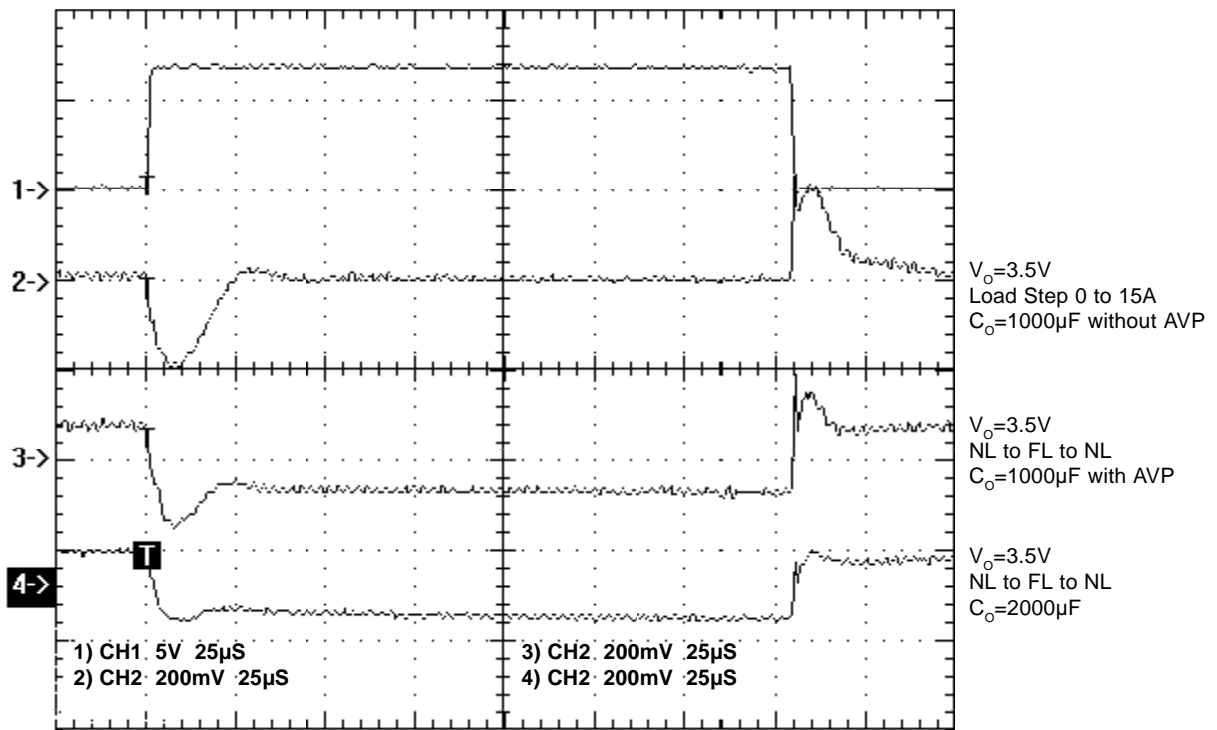


FIGURE 8. Active Voltage Positioning (AVP)

NOTE: The overshoot and undershoot are reduced or eliminated with AVP Traces 3 and 4 respectively.

APPLICATION INFORMATION

The SR50 is a 15A VID programmable step-down DC/DC converter. High switching frequency and synchronous rectification allows the converter to offer high efficiency in a small package. It

offers six different VID codes and operates from 2.5V to 12V input supply. Three different modes of operation allow for design flexibility.

PIN DESCRIPTION

Current Share (CSH) or Active Voltage Positioning (AVP) (Optional) (Pin 1): can be used for current share in multiple parallel-connected SR50 converters. AVP will perform active deregulation to preset the output voltage in applications that have high load step (see AVP).

Power Good (PG) Pin 2: An open collector output signal. Active low is pulled low if the output is not within $\pm 8\%$ of V_{OUT} or one of the following will occur: input overvoltage, short circuit and thermal protection. Depending on the output capacitors the time required for PG to go high is between 2.5 to 3.5mS. During active voltage transition of VID Code, PG can be momentarily activated.

VID0 thru **VID4** (Pins 3 thru 7): Digital inputs for controlling the output voltage of the converter. The VID inputs through the internal D/A converter can set the output to 32 discrete levels, as shown in Tables 1 thru 3. The internal D/A converter is a special D/A converter and the LSB represents different increments depending on the specific model and selected VID code.

ON/OFF (Pin 8): When this pin is pulled low, the converter is OFF. The converter is ON when Pin 8 is left open, and is OFF

when it is pulled low. When Pin 8 is low, the soft start capacitor of the PWM is discharged and the Power Good pin is also pulled low. The common cathode of an internal Schottky diode is connected to Pin 8 to allow for multiple SR50 ON/OFF connections. When the low level of the driver signal that is to be used for the ON/OFF is higher than 0.5V, use an open drain low-power MOSFET.

SYNC (Pin 9): Digital input signal to synchronize the switching frequency of the converter to an external clock. When external sync is used, the current sinking capability of the converter is deactivated (see Modes of Operation).

+V_{IN} (Pin 10 thru 12): Positive input voltage pins rated at 5A each.

-S V_{OUT} (Pin 13): Negative sense pin for the internal error amplifier is connected to $-V_{OUT}$ at the load end.

GND (Pins 14 thru 18): Ground pins for both V_{IN} and V_{OUT} .

+V_{OUT} (Pins 19 thru 22): Output voltage pins.
+S V_{OUT} (Pin 23): Positive output sense pin. Connected to $+V_{OUT}$ at the load end and can also be used for output current limit (see Output Current Limit).

MODES OF OPERATION

1) Continuous Mode – In Continuous Mode, the synchronous rectifiers continually switch at the specified frequency and will permit the output of the converter to sync and source current for applications such as DDR RAM 1.25 reference supply. All standard SR50 converters have the SYNC pin internally pull low, which forces the PWM to operate in Continuous Mode.

2) Burst Mode – Burst Mode improves efficiency at light loads by delivering power to the load in bursts. Burst Mode also increases the output ripple. In this mode, the SR50 will source only Current

External Clock Mode. When the SR50 is driven by an external system clock, the converter only sources current to the load. This mode of operation may be used in multi-converter parallel operations where the probability exists that one of the converters will sink current from the others at turn ON. For multiple converter operation, we recommend 50% duty cycle, 2-clock signal (Q and Q) to be connected to sequential converters in order to reduce input and output ripple, and external capacitance stress.

OVERVOLTAGE CROWBAR

When the output exceeds the nominal V_{OUT} by 8%, the PWM turns the top transistor OFF and the bottom ON in an attempt to reduce the overvoltage. It is strongly recommended to

use the specified input fuse in case the crowbar is activated and the top transistor is shorted.

SHORT CIRCUIT PROTECTION

The SR50 utilizes the parasitic resistance of the power pins and PCB traces to sense the output current. For a maximum 15A output current, the maximum parasitic resistance is given by $R_p = 0.05/15 = 3.3m\Omega$. Therefore, the maximum parasitic resistance R_p must be less than or equal to $3.3m\Omega$ from the converter's PCB to the load or where the +S pin is connected. For a 1/4-inch wide, 2-oz. copper trace, the distance from the converter to the load is approxi-

mately 1.5 inches. When the load is located more than 1.5" inches away, use a multilayer PCB or have the power traces plated up to 3 or 4 oz. If lower than 15A is required, a series resistor can be inserted in the positive trace, and the +S pin connected after the resistance at the load end. Keep in mind that Current Sense Resistance (R_s) is the sum of the discrete resistor and the parasitic trace resistance and that the parasitic resistance has high positive T.C.

Options

OPTION A: ACTIVE VOLTAGE POSITIONING (AVP)

Point of load (POL) step-down converters are used to power microprocessors and must maintain their output voltages within $\pm 0.1V$ or lower of the nominal V_O in spite of high-load current steps. The microprocessor or CPU can switch within 100nS from no load to full load. Because the feedback loop of the POL converter cannot keep up with the switching speed of the CPU, the input and output capacitor will provide the current during the switching of the load (CPU) until the POL converter can respond to the load demands.

When AVP is incorporated in a POL converter, it forces the point of load to set its output a few millivolts higher from V_{OUT} Nominal at light load and few millivolts lower at heavy load. AVP reduces the over/under shoot of the output, thus allowing for lower C_O (see Figure 7).

Below is given a step-by-step procedure to calculate the values of R_X, R_Y when AVP option is specified. Some of the constants are derived from semiconductor specifications.

The designer must know the maximum I_O required:
E_O = Error transconductance amplifier output

$$E_o \text{ Max} = [(1.15I_o) * 0.8] + 0.3V$$

$$E_o \text{ Min} = 0.4V$$

$$A_{E_o} = \text{gain of the error amplifier} = (E_o \text{ Max} - E_o \text{ Min}) / 0.06$$

$$R_{E_o} = \text{required gain equivalent resistor to set the gain} = R_x / R_y = A_{E_o} / 0.0013$$

$$V_o \text{ Nominal} = (E_o \text{ Max} - E_o \text{ Min}) / 2 + E_o \text{ Min}$$

$$\text{Calculate the constant: } N = (V_{IN} - E_o \text{ Nominal}) / E_o \text{ Nominal}$$

$$\text{then: } R_x = (N+1) * R_{E_o}, R_y = R_x / N$$

OPTION B: LATCHED SHORT CIRCUIT

When an overcurrent condition or short circuit output is present at the output, the PWM enters into shutdown mode by discharging the soft start capacitor and turns both transistors OFF. If the same condition exists at turn ON, the converter will go through its soft start phase; and if the output remains below 65% of V_{OUT} Nominal, the converter will go into shutdown latched off mode. To override the latched off condition, the input power must be recycled.

OPTION C: SKIP MODE ("BURST" MODE)

A converter with Option C at light loads will switch at "bursts," thus improving efficiency. Burst mode operation results in higher output ripple and noise.

OPTION D: OUTPUT CURRENT SHARE

When an output current higher than a single converter can provide is required by the load, multiple SR50 converters can be used. By connecting the C-SH (Pin 1) together, the converters are forced to share the output current by forcing the transconductance error amplifiers to current share. For best performance, use an external clock for synchronization as recommended in the External Clock Mode Section.