



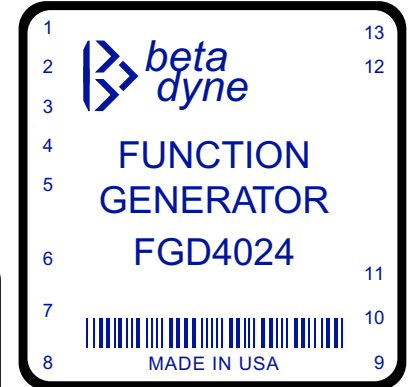
# FGD4024, FGD4048 & FGD4000

## FUNCTION GENERATORS

Programmable Frequency and Amplitude

### Key Features

- DC, sine, square and triangular wave outputs
- Double-buffered digital inputs w/Schmitt trigger
- Programmable frequency & amplitude
- 3-port SPI compatible microprocessor
- 12-bit multiplying DAC
- 1.2Hz, 2.44mV resolution
- DC to 40kHz
- 60µA off state current
- Hot pluggable
- Internal DC/DC converter
- 5W of auxiliary output power



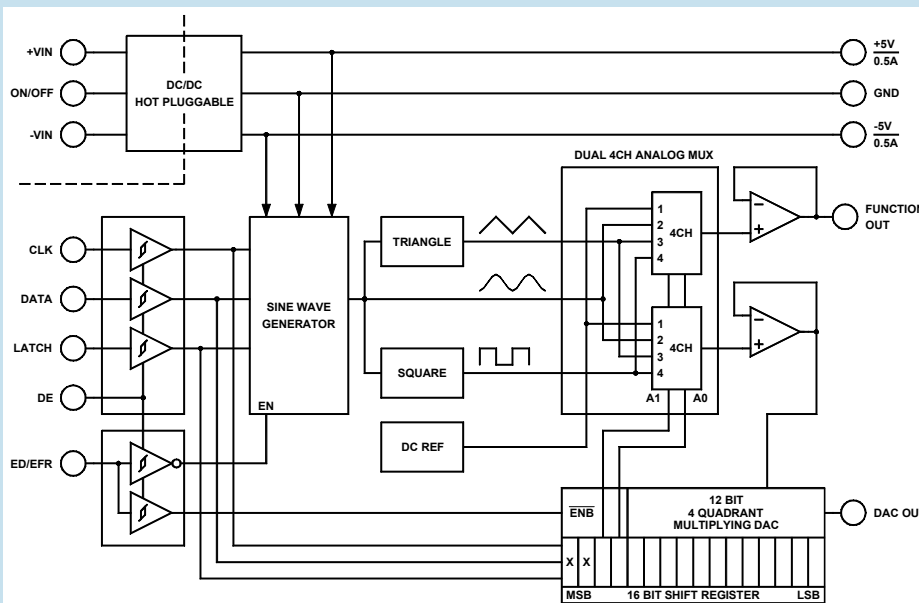
Beta Dyne is protected under various patents, including but not limited to U.S. Patent numbers: 5,777,519; 6,188,276; 6,262,901; 6,452,818; 6,473,3171.

### Applications

- AM/FM Modulation
- Telecom, Modem, Fax
- Test Pattern Generator
- Pseudo Random Noise Generator
- Test and Measurement
- Uninterruptible Power Supply
- Automatic Test Equipment

### Functional Description

The FGD40 series of function generators consist of three models. The FGD4024 and FGD4048 are packaged in a 2×2×0.395-inch case with internal DC/DC converters. The FGD4000 is packaged in a 2×1×0.395-inch case and requires a ±5V<sub>OUT</sub> supply. All models provide DC, sine, square and triangular wave outputs; and all four functions are software selectable and programmable with 1.2Hz frequency and 2.44mV amplitude resolution. The 12-bit multiplying DAC can perform multiplication of any selected function with its input data code.



$$f_o = \frac{f_{\text{CLOCK}} (D_{15} - D_0)_{\text{DEC}}}{2^{23}}$$

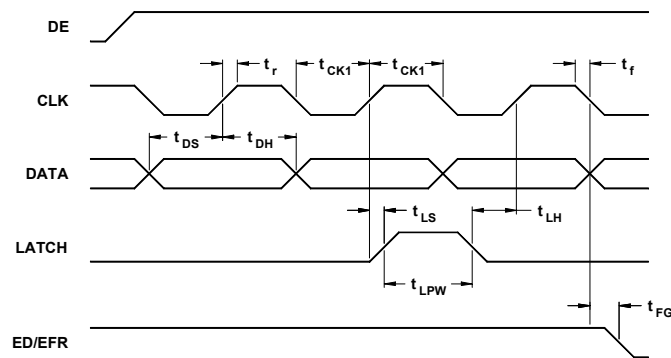
$$\text{DAC}_{\text{OUT}} = fX \frac{(D_{12} - D_0)_{\text{DEC}}}{2^{11}}$$

(fX = selected function)

Unless otherwise specified, all parameters are given under typical +25°C with nominal input voltage and under full output load conditions.

## INPUT LOGIC

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Maximum Positive-going Input Threshold	$V_{OUT} = 0.1V, I_O \leq 20A$		3.15		Vdc
Minimum Positive-going Input Threshold	$V_{OUT} = 0.1V, I_O \leq 20A$		2.25		Vdc
Maximum Negative-going Input Threshold	$V_{OUT} = V_{CC} - 0.1V$		2.05		Vdc
Minimum Negative-going Input Threshold	$V_{OUT} = V_{CC} - 0.1V, I_O \leq 20A$		0.90		Vdc
Maximum Hysterisis Voltage	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$		2.25		Vdc
Minimum Hysterisis Voltage	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V, I_O \leq 20A$		0.40		Vdc
Clock On/Off Period, $t_{CLOCK}$	See Serial Interface Timing	100			nS
Data Setup Time, $t_{DS}$		50			nS
Data Hold Time, $t_{DH}$		50			nS
Latch Pulse width, $t_{LPT}$		50			nS
Latch Hold Time, $t_{LH}$		50			nS
Latch Setup Time, $t_{LS}$		50			nS
DAC/Frequency ED/EFT+FG		50			nS



Serial Interface Timing

## OUTPUT WAVEFORMS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Total Harmonic Distortion, 20Hz to 5kHz	See Note 1		0.14	0.17	%
Total Harmonic Distortion, 5kHz to 25kHz	See Note 1		0.30	0.70	%
Total Harmonic Distortion, 25kHz to 40kHz	See Note 1		0.80	1.00	%
Gain Error, 20Hz to 5kHz	See Note 1			±0.15	dB
Gain Error, 5kHz to 25kHz	See Note 1			±0.30	dB
Gain Error, 25kHz to 40kHz	See Note 1, (See App. Note FG-001)			±0.60	dB
Offset Voltage				6.6	mV
Output Voltage Swing, Sine wave $\pm V_{CC}/2$			±2.5		Vdc
Output Voltage Swing, Triangle wave $\pm V_{CC}/2$			±2.5		Vdc
Output Voltage Swing, Square wave $\pm V_{CC}/2$			±2.5		Vdc
Slew Rate	$R_L = 2k, C_L = 500pF$		±13		V/μS
Output Frequency	User programmable	0	20	40	kHz
Output Current	Any waveform output		3		mA
Short Circuit Current	Any waveform output		10		mA

TABLE 1. Output Function Truth Table

Bit 14	Bit 13	$F_{OUT}$	$DAC_{OUT}$ Range
0	0	+2.5V	$-2.5 < V_O < 2.5$
0	1	Sine	Sine $-2.5 <-> 2.5$
1	0	Triangle	Triangle $-3 <-> 3$
1	1	Square	Square $-2.5 <-> 2.5$

TABLE 2. Bipolar (Offset Binary) Code Table  
( $-V_{REFIN}$  to  $+V_{REFIN}$  Output)

Input	Output
1111 1111 1111	$(+V_{REFIN})(2047/2048)$
1000 0000 0001	$(+V_{REFIN})(1/2048)$
1000 0000 0000	0V
0111 1111 1111	$(-V_{REFIN})(1/2048)$
0000 0000 0001	$(-V_{REFIN})(2047/2048)$
0000 0000 0000	$(-V_{REFIN})(2048/2048) = -V_{REFIN}$

## DAC Section

With DEVICE ENABLE (DE) high and ENB DAC/ENB FRQ (ED/EFR) high, the DAC's 16-bit shift register is activated. The two first bits 16, 15 of the register are dummy bits followed by bits 14, 13 which are the address bits of a dual 4-channel analog multiplexer (See Table #1). Then the following 12 bits (MSB to LSB) are the data bits of a 12-bit multiplying DAC. Data is clocked in on CLK's rising edge while LATCH is low. On LATCH's rising edge, the 12 least significant bits are transferred to the DAC register and updates the DAC. While LATCH is high, data cannot be clocked

into the DAC. The 4-to-1 dual analog multiplexer feeds one of the selected functions to the DAC reference input pins while the other channel is the function output pin of the generator. The reference input to the DAC signal is multiplied by the input DAC data and their product is the DAC<sub>OUT</sub> signal pin. The 12-bit DAC is set up to operate in the bipolar mode (offset binary) where the MSB is the sign bit followed by 11 binary weighted bits to produce an output within +DAC reference to -DAC reference. The DAC output is given in Table 2.

### DIGITAL TO ANALOG CONVERTER (DAC)

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Resolution		12			Bits
Relative Accuracy	$V_{CC} = 5V, V_{SS} = -5V$			±1	LSB
Differential Non-linearity	Guaranteed monotonic			±1	LSB
Bipolar Offset Error				±8	LSB
Bipolar Offset Temperature Coefficient			3		ppm/°C
Gain Error	Dual			±1	LSB
Gain Error Temperature Coefficient			1		ppm/°C
Power Supply Rejection Ratio (See Note 3)	$4.5V \leq V_{DD} \leq 5.5V, -5.5V \leq V_{SS} \leq -4.5V$		0.4	1	LSB/V
Output Voltage Range		-3		+3	Vdc

## DC/DC Converter Section

### INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Supply Voltage Range, FGD4024		18	24	36	Vdc
Supply Voltage Range, FGD4048		36	48	75	Vdc
Input Current, No Load, FGD4024			45		mA
Input Current, No Load, FGD4048			30		mA
Input Current, Full Load, FGD4024			290		mA
Input Current, Full Load, FGD4048			142		mA
Short Circuit Current		10	20	30	mA
Input Reflected Ripple, FGD4024			100		mA <sub>pp</sub>
Input Reflected Ripple, FGD4048			50		mA <sub>pp</sub>
Start-up Threshold			10		Vdc
Under Voltage Shutdown			10		Vdc
Input Filter Type	LC Filter				
Off State Input Current, FGD4024			60		µA
Off State Input Current, FGD4048			60		µA
Remote On/Off Control, ON	Pin 7 open, 10Vdc@100µA, internal pullup				
Remote On/Off Control, OFF	Jumper Pin 7 to -V <sub>IN</sub>				
Case Connection, FGD4024	-V <sub>IN</sub>				
Case Connection, FGD4048	+V <sub>IN</sub>				

### OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Voltage		±4.75	±5.00	±5.25	Vdc
Voltage Imbalance				3	%
Output Current		10	500	500	mA
Short Circuit Protection	Indefinite				
Load Step Response	50% to FL, FL to 50% to 0.1% of V <sub>OUT</sub>		100	200	µS
Turn On Delay			8		mS
Output Ripple & Noise	20MHz bandwidth (See App. Note FG-001)		50	100	mV <sub>pp</sub>
Load Regulation	Minimum to FL			1	% of V <sub>OUT</sub>
Line Regulation	Minimum to maximum input voltage			1	% of V <sub>OUT</sub>
Temperature Coefficient	Nominal line, FL		±0.01	±0.02	%/°C
Efficiency	FL including 0.5W for internal circuits		80		%
Derating	No derating -40°C to +85°C				

## GENERAL SPECIFICATIONS

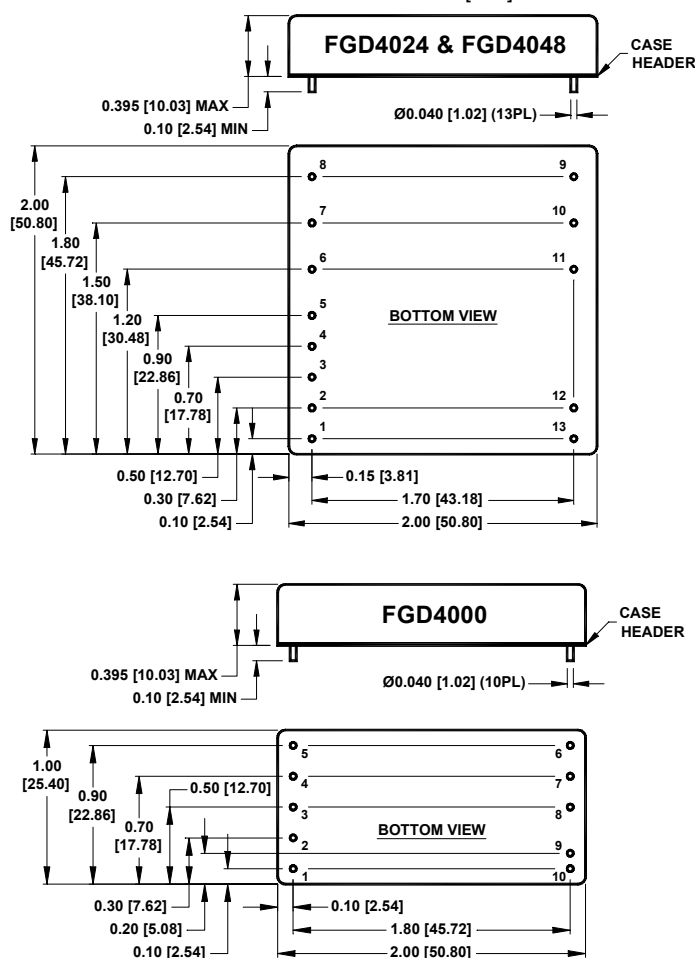
PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Switching Frequency		110	120	125	kHz
Isolation Voltage		1000	1500		V <sub>RMS</sub>
Isolation Resistance			10 <sub>9</sub>		Ω
Thermal Resistance	Case to ambient	1	2		°C/W
MTBF	per MIL-HDBK-217F (Ground benign, +25°C)		1×10 <sup>6</sup>		hours

## ENVIRONMENTAL / PHYSICAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Humidity	Non-condensing			95	%
Storage Temperature		-60		+125	°C
Operating Temperature, Commercial		-40		+75	°C
Operating Temperature, Extended	Contact factory for price and availability	-55		+85	°C
Dimensions, FGD4024 & FGD4048 (L×W×H)	2.00×2.00×0.395 in. (50.80×50.80×10.03mm)				
Dimensions, FGD4000 (L×W×H)	2.00×1.00×0.395 in. (50.80×25.40×10.03mm)				
Weight, FGD4024 & FGD4048	2 oz. (58g)				
Case Material	Coated metal; Six-sided shielding				
Header	FR-4, non-conductive				
Potting	Thermally conductive				

### MECHANICAL SPECIFICATIONS

in inches [mm]

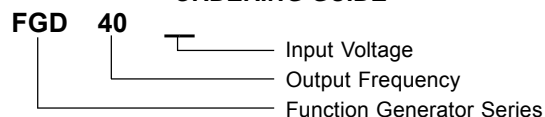


See App. Note FGD-001 for Typical Connection Diagram

### FGD4024 & FGD4048

Pin	Function	Pin	Function
1	LATCH	9	+5V
2	DATA	10	GND
3	CLK	11	-5V
4	ED/EFR	12	DAC <sub>OUT</sub>
5	DE	13	FUNCTION <sub>OUT</sub>
6	-V <sub>IN</sub>		
7	ON/OFF		
8	+V <sub>IN</sub>		

### ORDERING GUIDE



### MODEL CHART

Model	Output Frequency	Input Voltage	Output Voltage
FGD4024	40kHz	24Vdc	±5Vdc
FGD4048	40kHz	48Vdc	±5Vdc
FGD4000	40kHz	±5Vdc	None

### FGD4000

Pin	Function	Pin	Function
1	LATCH	6	+5V
2	DATA	7	GND
3	CLK	8	-5V
4	ED/EFR	9	DAC <sub>OUT</sub>
5	DE	10	FUNCTION <sub>OUT</sub>

## NOTES

1. Converting THD from % to dB: THD in dB = (THD in %) / 100
2. To measure offset voltage, put the Function Generator in sleep mode and measure the sine and triangular wave output voltage. The square wave output will be between +V<sub>CC</sub> and -V<sub>CC</sub>.
3. Specifications are subject to change without notice.
4. All specifications are typical @ +25°C with nominal input voltage and under full power conditions, unless otherwise noted.